F-24314C2

#8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: JOSEPH T. EVANS, JR., ET AL.

Serial No.: 582,672
Filed: September 14, 1990
Group: 233
Examiner: Alyssa H. Bowler
For: NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

DECLARATION OF WILLIAM D. MILLER

I, William D. Miller, of 160 Mobray Court, Colorado Springs, Colorado 80906, do hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, do hereby declare as follows:

1. I began working for Krysalis Corporation on or about March, 1985, as Manager of Process Development. I later became Vice President, and then President of Krysalis Corporation.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 8, 1991 (Date of Deposit)

Roger N. Chauza, Reg. No. 29,753
Name of applicant, assignee, or Registered Representative

Signature

July 8, 1991
Date of Signature

During my tenure with Krysalis Corporation, I was integrally involved with the development efforts of a ferroelectric material suitable for use in solid state memory circuits. Because Krysalis Corporation was a small corporation, I had personal knowledge of the development responsibilities and efforts of the employees of the corporation in this endeavor.

2. Krysalis Corporation was founded for the purpose of developing techniques for integrating ferroelectric material with silicon circuits using semiconductor processing technology. The charter of Krysalis was to develop a ferroelectric material for thin film deposition onto semiconductor wafers to form microelectronic nonvolatile devices. To the best of my knowledge, previous to the 1986 time period, no one had ever successfully developed a ferroelectric material which could be applied as a thin film to silicon wafer circuits, using known semiconductor processing techniques and apparatus.

3. A three-part goal of Krysalis Corporation was to develop a ferroelectric material which could be deposited as a thin film on silicon, without contaminating the silicon material. An associated goal of Krysalis Corporation was to develop an improved composition of ferroelectric material that exhibited reduced fatigue and aging characteristics as compared to prior ferroelectric material, and thus adapted for memory applications. Another major and related goal of Krysalis Corporation was to develop processing techniques so that large arrays of non-volatile memory cells, utilizing ferroelectric capacitors and CMOS transistors, were made commercially feasible.

4. A primary impediment to the achievement of the foregoing goals was that the useful life of traditional ferroelectric material was limited, and thus not readily usable in memory circuits. Another substantial impediment to the integration of ferroelectric material with silicon circuits, was that the processing temperatures required by the ferroelectric material were well above that utilized in processing silicon wafers to fabricate transistor circuits therein. As a result, when depositing an amorphous ferroelectric material on a silicon circuit wafer and sintering the ferroelectric material to form a Perovskite crystalline material that is polarizable, the high temperature processing steps tended to destroy or degrade the semiconductor transistor junctions.

5. An initial undertaking of Krysalis Corporation was the development of a ferroelectric, thin film composition which could be deposited on silicon material without substantial adverse effects thereon, and which exhibited better fatigue and aging characteristics over other well known compositions, such that it could be used in semiconductor memories. As it turned out, the development of a ferroelectric, thin film composition by Krysalis Corporation spanned the years of at least 1986 through 1989.

6. The ferroelectric material comprises the dielectric material that is formed between two conductive surfaces to define the ferroelectric capacitor. The ferroelectric capacitor itself is a component of the nonvolatile memory cells developed and commercialized by Krysalis Corporation. More particularly, the ferroelectric capacitor is a component of the non-volatile memory cell that is disclosed and claimed in the captioned continuation patent application.

7. On information and belief, the parent patent application, of which the above-captioned application is one of a number of continuations, was initially assigned to Krysalis Corporation. By way of various subsequent assignments, the above-captioned continuation application is believed to be presently assigned to National Semiconductor Corporation of Santa Clara, California.

8. A further impediment to the integration of ferroelectric capacitors with silicon wafer technology was that ferroelectric capacitor structures of that time required an operating voltage substantially higher than that utilized by conventional semiconductor memories and associated circuits.

9. In order to develop and evaluate ferroelectric compositions and materials, Krysalis Corporation developed ferroelectric capacitor test structures on silicon wafers. Exhibit 1 is a copy of a Krysalis document that pictorially illustrates a test structure for ferroelectric capacitors formed on a silicon wafer for testing fatigue of the ferroelectric material. Fatigue is the degradation over time of the ability of the ferroelectric material to maintain the original magnitude of the polarization states. Fatigue is caused by the AC cycling or switching of the polarization states of a ferroelectric capacitor from one state to the other. The ferroelectric material has a characteristic hysteresis loop, giving it the ability to store polarization states without power being applied to the capacitor, thereby giving it the ability to maintain one or the other of the polarization states in a non-volatile manner.

10. Exhibit 2 is a Krysalis process and test document having a form and format of which I am familiar and recognize. Exhibit 2 shows the results of fatigue tests of a wafer identified as F6119. The test results are tabulated with numerical data, as well as graphs of various capacitor parameters. The graphs show the capacitor parameters on a vertical scale of microcoulombs/square centimeters versus the number of switching cycles to which the capacitor was subjected. Such capacitor test structures were utilized by Krysalis throughout the 1986 and 1987 time frame for testing various ferroelectric compositions for fatigue as well as other parameters.

11. Exhibit 3 is a Krysalis document that illustrates the process flow for fabricating a ferroelectric capacitor on a silicon semiconductor circuit. The process flow illustrates those steps which were carried out by Krysalis on TDO1 test wafers, which wafers had CMOS transistor circuits. A number of masks were developed by outside vendors so that the ferroelectric capacitor structures could be fabricated at particular wafer areas, and interconnected with the underlying transistor circuits.

The Krysalis capacitor fabrication process, as noted in Exhibit 3, involved an initial low pressure chemical vapor deposition of a nitride on the silicon wafer to form an insulating silicon nitride layer. The bottom electrode (BEL) of the capacitor was formed by sputtering on the silicon nitride other layers of titanium and platinum. The ferroelectric dielectric material was then deposited on the bottom electrode. The ferroelectric material, defining the dielectric of the capacitor, was made by forming a number of thin films to define a composite dielectric layer. The top electrode (TEL) of the ferroelectric capacitor was then deposited and patterned by etching. The underlying

ferroelectric material was also etched. The underlying silicon nitride was also patterned and etched. Aluminum contacts were then deposited and patterned.

12. Krysalis Corporation first developed techniques for integrating ferroelectric capacitors with silicon transistor circuits on test wafers, termed "TDO1" wafers. Krysalis Corporation retained an outside vendor, Orbit Semiconductor, Inc., of Sunnyvale, California, to supply the mask sets and to fabricate the silicon circuits in the semiconductor material. Exhibit 4 are copies of invoices and purchase order acknowledgements from Orbit Semiconductor, which documents identify the conversion of tape data and the fabrication of TDO1 wafers during September of 1986. Each die of the TDO1 wafer included a 2x2 array of memory cells employing ferroelectric capacitors and MOS transistors to provide non-volatile storage of data. Mr. Womack's Declaration, which accompanies this material, is believed to identify and describe the particular structure and operation of the non-volatile ferroelectric memory cells.

13. A ferroelectric capacitor constitutes a circuit component of the non-volatile memory cell, as well as a component used in other types of memory cells that were planned to be developed, and were indeed developed in silicon wafers by Krysalis Corporation during 1986 and 1987. The development of a ferroelectric capacitor adapted for integration with transistor circuits on a semiconductor wafer required substantial additional development by Krysalis Corporation. The development by Krysalis of an integrated ferroelectric capacitor itself continued throughout 1987, in parallel with the development of other ferroelectric memory circuits and test structures.

14. Exhibit 5 constitutes a number of copies of documents from Orbit Semiconductor, Inc. dated between January 15, 1987, and June 15, 1987. These documents are order acknowledgements, packing slips and invoices verifying the preparation of wafer processing masks and the preparation of ECD512 CMOS wafers themselves. It is believed that Master Images, Inc. fabricated the masks for Orbit Semiconductor. Some of the masks of the various sets were utilized by Orbit Semiconductor to fabricate the transistor circuits in the silicon wafers, and thereafter, Krysalis Corporation utilized the remaining masks to deposit the various layers of material, including ferroelectric material, to define capacitors connected to the transistor circuits. It is further believed that some of the masks identified in the documents of Exhibit 5 were utilized to fabricate fatigue and other test structures for testing various ferroelectric films made by Krysalis.

15. Exhibit 6 is a packing list by Indy Electronics, Inc., a vendor that packaged ferroelectric chips for Krysalis. Essentially, Krysalis would prepare a ferroelectric material and deposit it as a thin film on a wafer. Krysalis would then mask the wafer and pattern the ferroelectric material to define the capacitor dielectric on each die of the wafer. Next, the wafers were sent to Indy Electronics, Inc. where the wafers were cut into the individual die and packaged by encapsulation. As noted in the packing list of Exhibit 6, Indy Electronics shipped 2,666, 16-lead, side brazed devices, each having a die cut from one of the three Krysalis-processed wafers, namely, wafer 7076A, 7076B or 7069D.

16. Exhibit 7 is a letter from Dino Asselanis, an employee of Krysalis Corporation, to Mr. John Sheets, a process engineering of ASM America, Inc. The letter is dated May 12, 1987, and describes 12 tests wafers prepared by Krysalis and to have a passivation layer deposited thereon by ASM America, Inc. The effects of the passivation as a function of the various film sandwich layers and the process temperatures were to be evaluated by Krysalis personnel.

17. Exhibit 8 is a copy of my memorandum dated June 22, 1987, and entitled "Technology Development Action Plan". Exhibit 8 illustrates the various areas in which the ferroelectric capacitor required further development. The further development efforts by Krysalis personnel of ferroelectric capacitors took place in 1987 in parallel with a "512" project and a "16K" project. The 512 and 16K projects involved the development of memory array structures, of which the cells were of a non-volatile type, employing ferroelectric capacitors. The 512 project provided a test structure by which the transistor circuits themselves could be tested, as well as a vehicle to test the performance of the ferroelectric capacitors. In tandem with the 512 and the 16K projects, ferroelectric structures similar to that illustrated in Exhibit 1 hereof, were further utilized to develop and assess the ferroelectric material for its adaptability to integration in silicon wafer circuits.

18. Exhibit 9 is an undated Krysalis document which illustrates in a more detailed manner the efforts undertaken by Krysalis Corporation in developing ferroelectric capacitor structures. It is my belief that all such matters were addressed by Krysalis personnel.

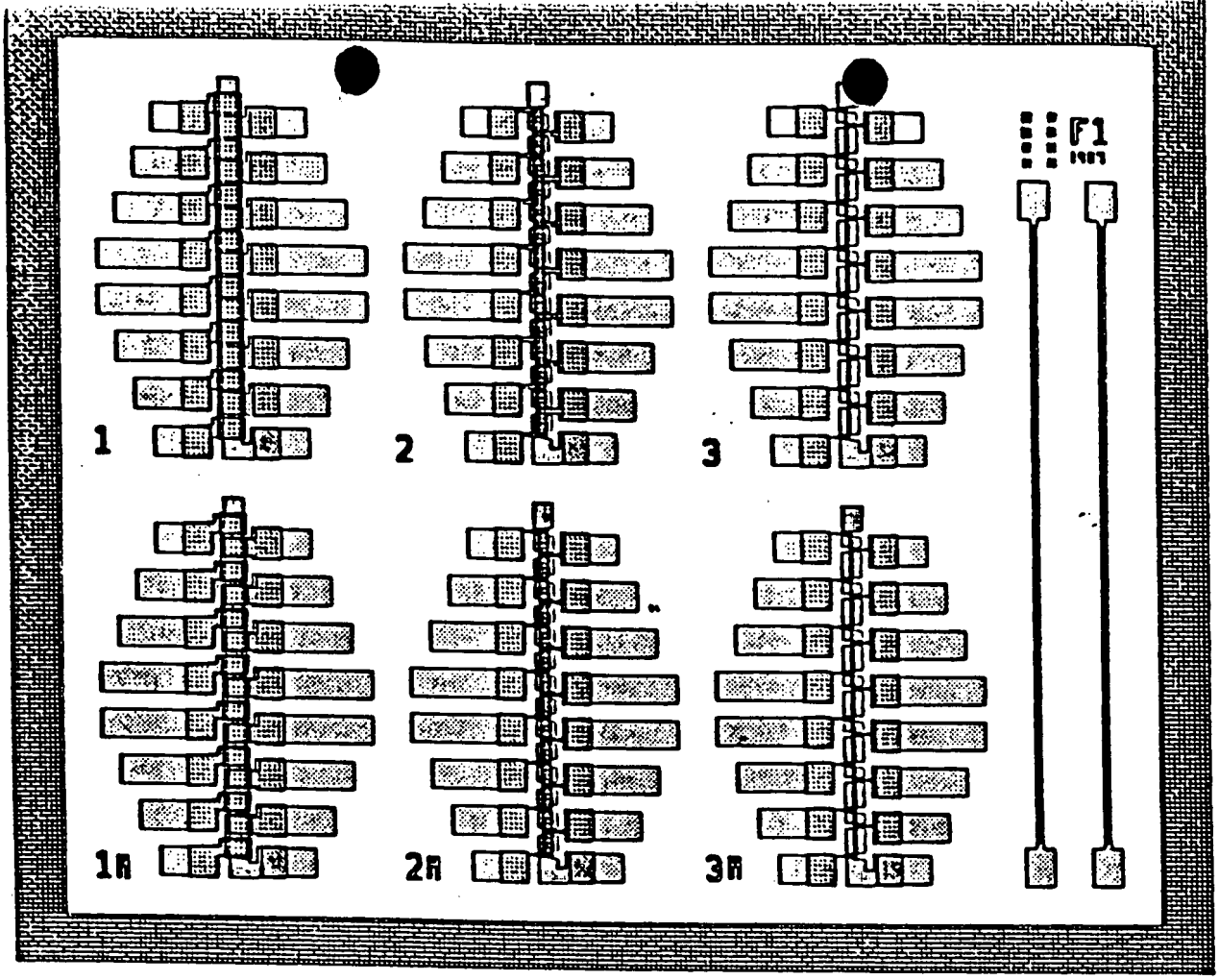
19. Exhibit 10 is a technical article, authored by employees of Krysalis Corporation, and believed to be published sometime in 1988. The article indicates that an experimental ferroelectric-based 512-bit random access memory was successfully developed. The 512-bit ferroelectric memory was developed for testing the suitability and electrical characteristics of ferroelectric material developed by Krysalis.

20. All the development and testing efforts by Krysalis Corporation and its employees were carried out in this country.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: July 1, 1991

William D. Miller



Above are the six different types of Fatigue structures. Below is a list of each structure, capacitor size and whether or not the structure has aluminum.

STRUCTURES	CAPACITOR SIZE	FINISHED STRUCTURE
1	100X100	W/O Aluminum
1A	100X100	W/Aluminum
2	20x20	W/O Aluminum
2A	20X20	W/Aluminum
3	9x5	W/O Aluminum
3A	9x5	W/Aluminum

Figure 13 - Test Structures for Measuring Ferroelectric Properties

FILM TEST WAFER TRAVELER

Film Log #: F6119

2

Comments

I. Substrate Preparation:

☐ Bulk Pt:
Surface Preparation: _____

☒ Thin Film: 1/4-B10
Approximate Oxide Thickness: 2700 Å
Pre-Clean: NONE
Bottom Metal Deposition Date: 7/1/86
Deposition Conditions:
Base Pressure: 2.3 E-6 torr
Heater Set Point: 250 °C

Ti/TiN/Ti/TiN/Ti/Pt
100/300/1000/300/150/900 Å

	Dep. Time (min.)	Press. (microns)	Power (W)
Ti:			
Pt:			

Estimated Thickness: Ti: _____ μ Pt: _____ μ

II. Solution Preparation:

Preparation Date: 29JUL86 Gel Log #: G621
Composition: 3 / 40 / 60 Excess Pb: 10 %

Starting Material Stock Number:
(date recieved - vendor code - unit designation)
Pb: _____-_____-__ Bu: _____-_____-__
Zr: _____-_____-__ Pr: _____-_____-__
Ti: _____-_____-__ Ac: _____-_____-__
La: _____-_____-__

Preparation Spec. Revision Used: _____

III. Film Deposition:

Deposition Date: 6-AUG-86 Number of Coats: 10
Pre-Clean: IPA RINSE/SPIN
Approx. Sol. Volume Dispensed: 0.2 ml
Approx. Spin Speed: 2000 RPM

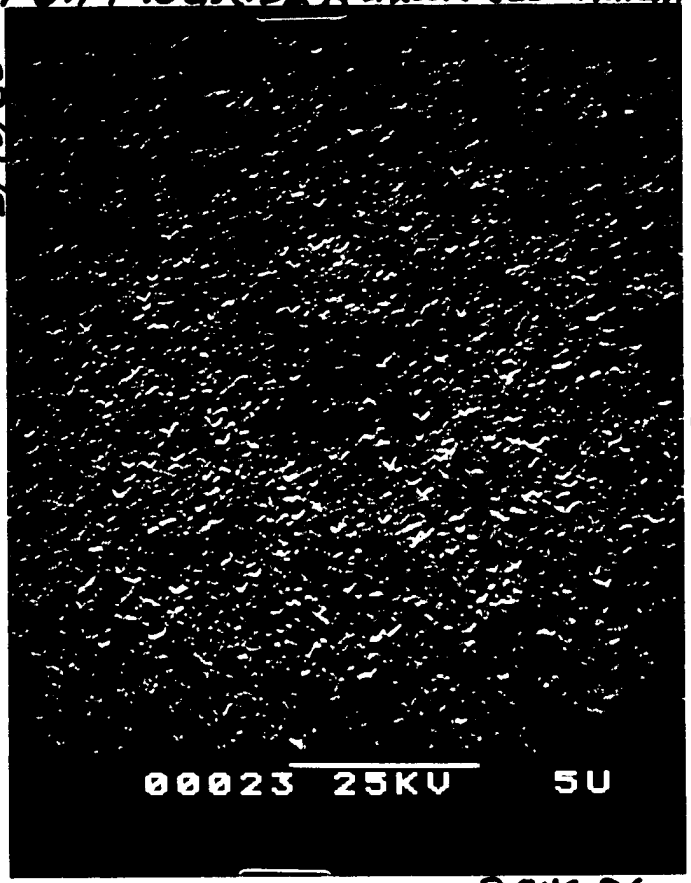
Minimized time film was in ambient humidity (room) by placing sample in boat in Tube #4 entrance immediately after spinning. SEM photos. Some metal/film blistering noted after anneal.

Sintering:
O_2 Flow: 2 l/min. Ramp Rate: 5 in/min.
Final Temp: 550 °C Time @ Temp: 10 min
Pull Rate: 5 in/min. Furnace Tube #: 4

Final Anneal:
O_2 Flow: 2 l/min. Ramp Rate: 10 in/min.
Final Temp: 625 °C Time @ Temp: 120 min
Pull Rate: 10 in/min. Furnace Tube #: 3

G621 on B10-5/550/5 SINTER
F6119-10 cts (.5U), 2 hour-625 ANNEAL

3/40/60

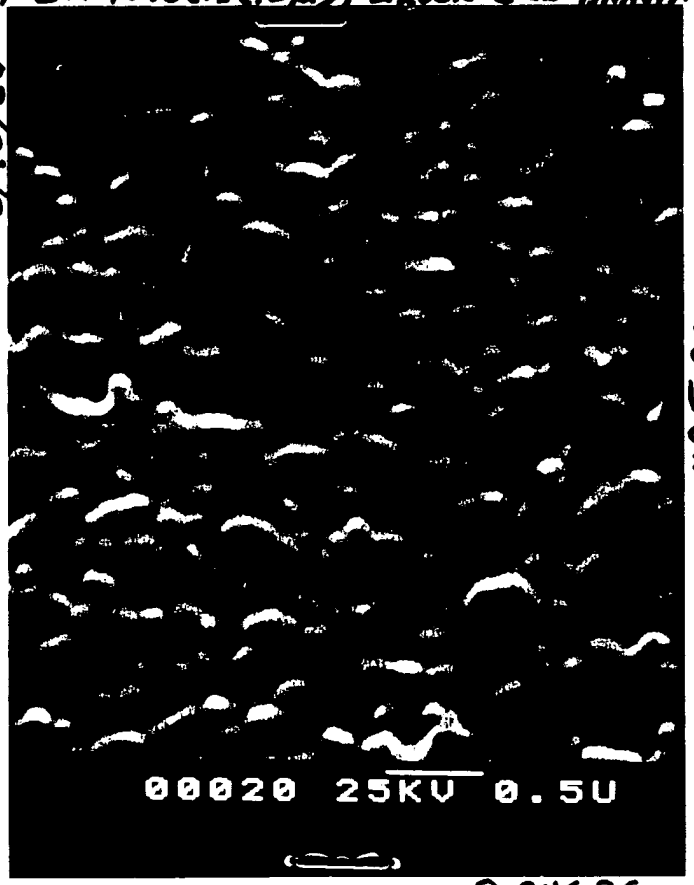


X5,000

8AUG86
LNC

G621 on B10-5/550/5 SINTER
F6119-10 cts (.5U), 2 hour-625 ANNEAL

3/40/60



X25,000

8AUG86
LNC

Comments

IV. Platinum Counter Electrode Deposition:

Deposition Date: 8/11/92 Shadow Mask #: 2

Deposition Conditions:

Pump-down + Pre-heat Total Time: 60 min.

Base Pressure: 1.2 E- 6 torr

Heater Set Point: RT °C

	Dep. Time (min.)	Press. (microns)	Power (W)
Ti:			
Pt:	2.5	9μ	170

Estimated Thickness: Ti: ____ μ Pt: ____ μ

N/O mark thickness would have been 1200 - 1300 Å. Actual thickness unknown.

V. Evaluation:

Ellipsometer:

Refractive Index: ____ Thickness: ____ μ

Average Measured Electrode Diameter: ____ μ

Electrical Characterization: Date Tested: ____

Test Set-Up Used: ____

Method Notes: ____

Assumed in Calculated Values:

Thickness: ____ μ Electrode Diam: ____ μ

Room Temperature / Ø Cycles Testing:

Measured Temperature: ____ °C

# of Good Capacitors: ____

# of Capacitors Tested: ____

Capacitor Yield: ____ %

Avg. Small Signal Capacitance @ 1KHz: ____ nF

RMS Deviation: ____

Avg. Small Signal Loss @ 1KHz: ____ %

RMS Deviation: ____

Calculated Small Signal Dielectric Constant: ____

P_r: ____ ($\mu C/cm^2$) P_r / P_s: ____

V_c: ____ (V) E_c: ____ (MV/m)

100°C / Ø Cycles Testing:

P_r: ____ ($\mu C/cm^2$) P_r / P_s: ____

V_c: ____ (V) E_c: ____ (MV/m)

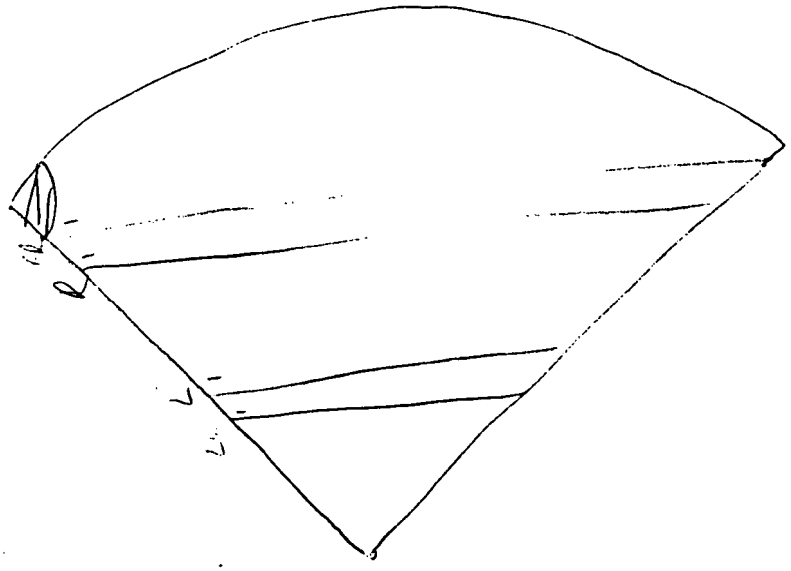
100°C / 10^9 Cycles Testing:

P_r: ____ ($\mu C/cm^2$) P_r / P_s: ____

V_c: ____ (V) E_c: ____ (MV/m)

Dektak Film Thickness Measurement: ____ μ

F 119



PCELL TESTING PROGRAM
Polarization Values
08-13-1986 16:27:48

Cell# 0 => RR6 Cell# 1 => L7

Csense = 9.25E-09

Probe # 0
Area = 7.853975E-05 cm^2
Batch# = G621
Process = 5/550/5/120@625
FLOG# = 6119
Composition = 3/40/60 W/10
Thickness = .5 microns
Cell Capacitance = 2.6823E-10 F

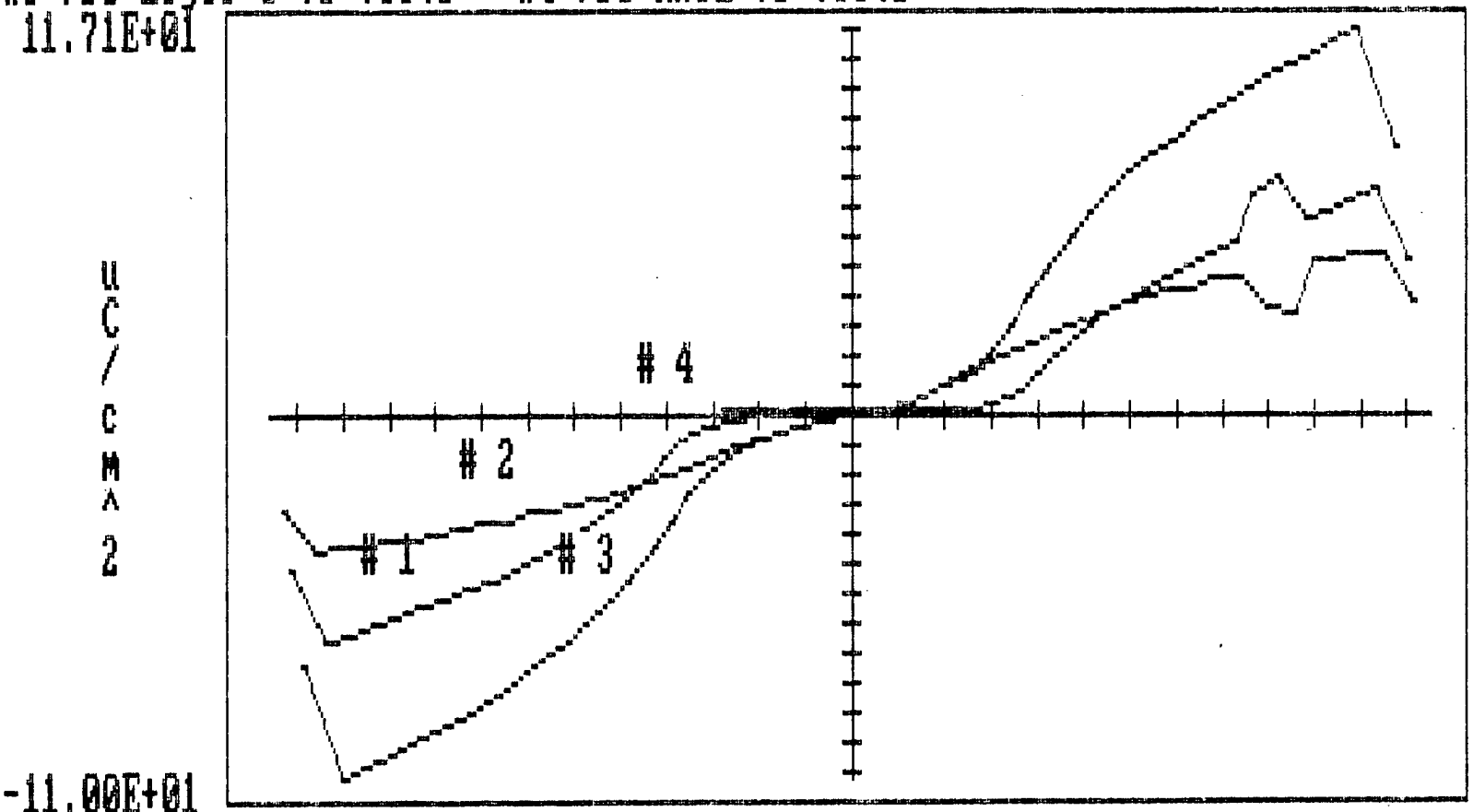
PROBE # 1
Area = 7.853975E-05 cm^2
Batch# = G621
Process = 5/550/5/120@625
FLOG# = 6119
Composition = 3/40/60 W/10
Thickness = .5 microns
Cell capacitance = 2.904E-10 F

Mode = PULSE
Trigger delay = .00002 secs

Probe# 0 Datafile = \MBYTE\DAT\P6119RR6.DO
Probe# 0 Infofile = \MBYTE\DAT\P6119RR6.IO
Probe# 1 Datafile = \MBYTE\DAT\P6119L7.DO
Probe# 1 Infofile = \MBYTE\DAT\P6119L7.IO

			Probe 0				Probe 1			
			+Prem ->	-Prem ->			-Prem ->	+Prem ->		
VclAq	Time	Temp	+Pset	-Pset	+Pdel	+RATL	-Pset	+Pset	-Pdel	-RATL
+12.667	16:28:03	+25	+33.0	-81.9	+47.0	+0.43	+58.4	+133.4	+75.0	+0.44
+11.548	16:28:25	+25	+49.5	+117.1	+67.7	+0.42	+56.4	+131.1	+74.8	+0.43
+10.984	16:28:45	+25	+47.7	+112.7	+65.0	+0.42	+54.6	+127.4	+72.7	+0.43
+10.465	16:29:16	+25	+46.9	+109.8	+61.9	+0.43	+52.9	+123.2	+70.3	+0.43
+10.062	16:29:36	+25	+46.1	+105.8	+59.7	+0.44	+51.8	+119.6	+67.9	+0.43
+9.516	16:29:56	+25	+30.9	+102.1	+71.2	+0.30	+49.6	+114.3	+64.8	+0.43
+8.952	16:30:16	+25	+31.9	+97.9	+65.9	+0.33	+47.5	+108.5	+61.0	+0.44
+8.495	16:30:36	+25	+41.1	+93.8	+52.7	+0.44	+45.9	+103.0	+57.1	+0.45
+7.904	16:30:56	+26	+40.5	+88.5	+47.9	+0.46	+43.6	+96.2	+52.6	+0.45
+7.439	16:31:16	+25	+36.5	+83.6	+45.0	+0.46	+41.2	+90.0	+48.8	+0.46
+6.956	16:31:36	+25	+37.6	+79.1	+41.5	+0.46	+38.8	+83.7	+44.9	+0.46
+6.445	16:31:56	+25	+35.2	+73.6	+38.4	+0.48	+36.8	+76.2	+39.4	+0.48
+6.042	16:32:17	+25	+33.4	+68.4	+35.1	+0.49	+34.5	+70.0	+35.5	+0.49
+5.496	16:32:37	+25	+30.9	+60.8	+29.9	+0.51	+31.5	+60.8	+29.2	+0.52
+5.058	16:32:57	+25	+28.7	+54.2	+25.5	+0.53	+28.8	+53.0	+24.2	+0.54
+4.404	16:33:17	+25	+25.2	+43.5	+18.3	+0.58	+25.0	+41.6	+16.6	+0.60
+3.984	16:33:37	+25	+22.1	+35.5	+13.3	+0.62	+21.9	+33.4	+11.4	+0.66
+3.572	16:38:14	+23	+19.5	+26.7	+7.3	+0.73	+16.6	+24.5	+5.9	+0.76
+3.008	16:38:47	+26	+15.3	+18.4	+3.1	+0.83	+15.1	+17.6	+2.5	+0.86
+2.444	16:39:07	+25	+11.2	+12.4	+1.2	+0.91	+11.6	+12.6	+1.0	+0.92
+1.943	16:39:27	+25	+8.3	+8.7	+0.4	+0.96	+8.4	+8.6	+0.2	+0.98
+1.493	16:39:47	+25	+5.5	+5.8	+0.3	+0.95	+6.0	+6.2	+0.2	+0.97
+1.233	16:40:07	+25	+4.3	+4.1	-0.2	+1.05	+4.3	+4.4	+0.1	+0.98
+0.600	16:40:27	+25	+2.0	+1.9	-0.1	+1.05	+2.4	+2.3	-0.1	+1.04

#1->D0 Delta P vs Volts #2->D0 Logic 1 vs Volts
#3->D0 Logic 0 vs Volts #4->D0 RAIL vs Volts

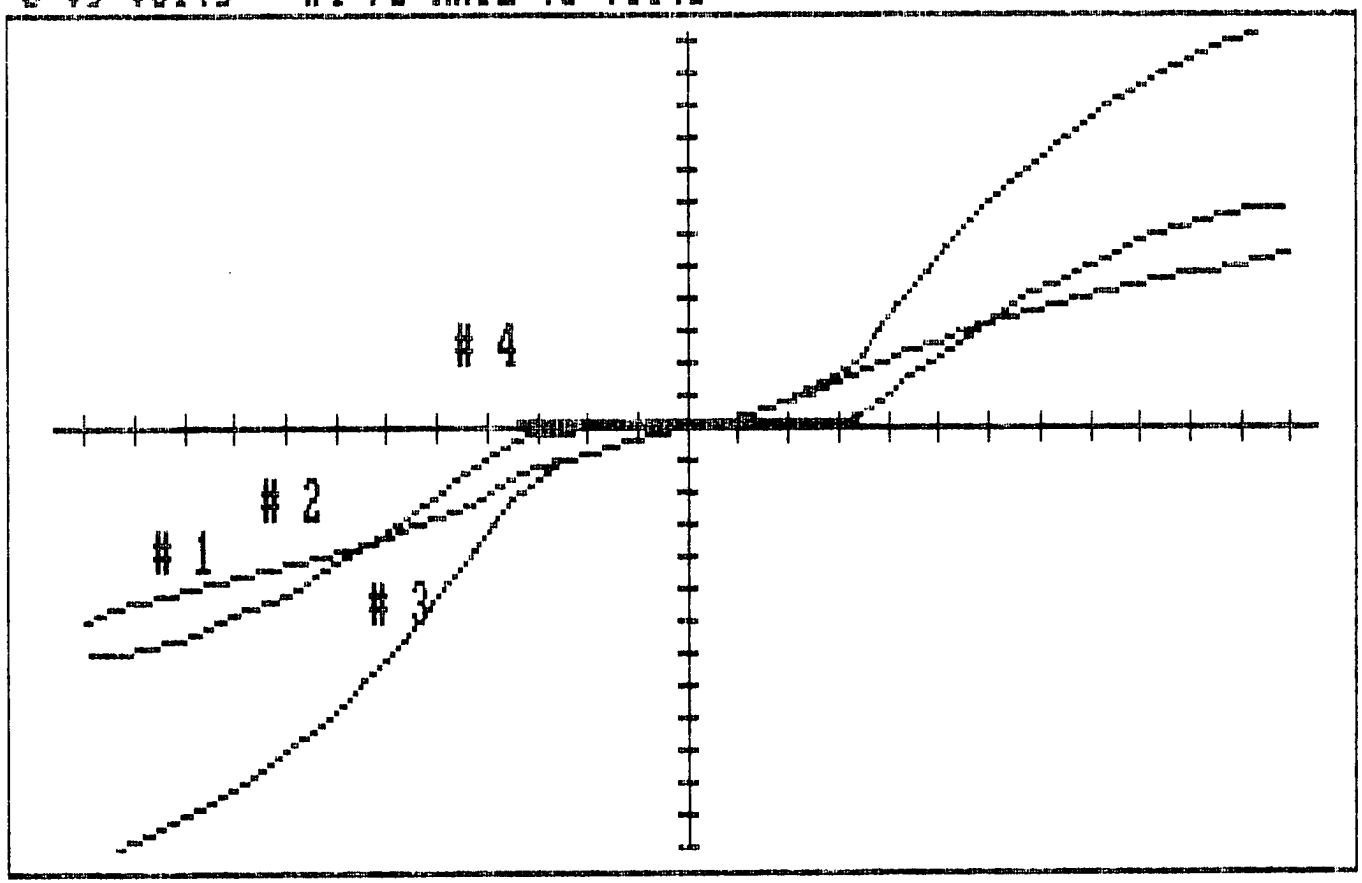


dX= 9.7E-01 dY= 9.0E+00 LINEAR / LINEAR 08-13-1986 16:42:24

Datafile = \MBYTE\DAT\P6119RR6.D0
Comp = 3/40/60 W/10 Thick = .5 microns 08-13-1986 16:40:52
Mode = PULSE Trigger time = .00002 secs Cap = 2.6828E-10

Cell appears to be over an area of bubbled epitaxt.
JE

#1->0 Delta P vs Volts #2->0 Logic 1 vs Volts
#3->0 Logic 0 vs Volts #4->0 RATL vs Volts



Temp: 25 C

dX= 9.7E-01 dY= 1.1E+01 LINEAR / LINEAR 08-13-1986 16:47:54

Datafile = \MBYTE\DAT\P6119L7.D0
Comp = 3/40/60 W/10 Thick = .5 microns 08-13-1986 16:41:09
Mode = PULSE Trigger time = .00002 secs Cap = 2.904E-10

PCELL TESTING PROGRAM
Polarization Values Cell# 0 => RR5 Cell# 1 => L8
08-13-1986 17:04:55

Csense = 9.25E-09

Probe # 0
Area = 7.853975E-05 cm^2
Batch# = 6621
Process = 5/550/5/120@625
FLOG# = 6119
Composition = 3/40/60 W/10
Thickness = .5 microns
Cell Capacitance = 3.274E-10 F

PROBE # 1
Area = 7.853975E-05 cm^2
Batch# = 6621
Process = 5/550/5/120@625
FLOG# = 6119
Composition = 3/40/60 W/10
Thickness = .5 microns
Cell capacitance = 3.8E-10 F

Mode = PULSE
Trigger delay = .00002 secs

Probe# 0 Datafile = \MBYTE\DAT\F6119RR5.DO
Probe# 0 Infofile = \MBYTE\DAT\F6119RR5.IO
Probe# 1 Datafile = \MBYTE\DAT\F6119L8.DO
Probe# 1 Infofile = \MBYTE\DAT\F6119L8.IO

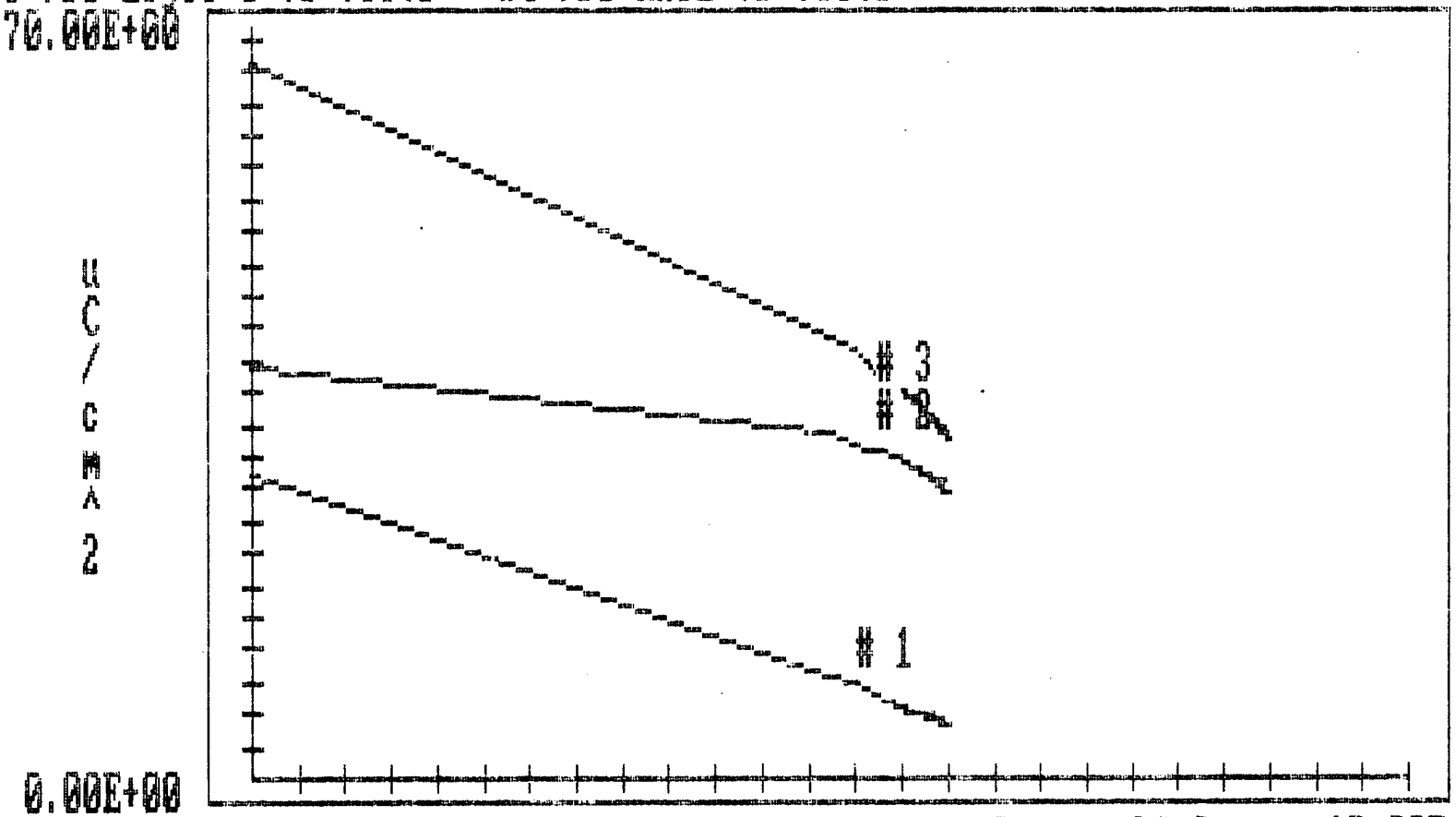
		Probe 0				Probe 1			
		+Prem ->	-Prem ->			-Prem ->	+Prem ->		
Cycles	Time	Temp	+Psat	+Psat	+Pdel	+RATL	-Psat	-Psat	-Pdel	-RATL
0.E+00	17:03:13	+95	+38.5	+66.6	+28.1	+0.58	+46.3	+82.6	+36.3	+0.56
3.E+07	17:06:14	+97	+32.0	+41.3	+9.3	+0.77	+39.6	+52.4	+12.7	+0.76
6.E+07	17:07:16	+97	+31.1	+39.8	+8.6	+0.78	+38.5	+50.1	+11.6	+0.77
7.E+07	17:08:17	+97	+30.8	+39.1	+8.3	+0.79	+38.5	+49.4	+10.8	+0.78
1.E+08	17:09:19	+98	+30.5	+38.1	+7.6	+0.80	+38.4	+48.4	+10.0	+0.77
2.E+08	17:10:20	+96	+30.3	+37.7	+7.4	+0.80	+37.2	+46.9	+9.7	+0.79
2.E+08	17:11:22	+98	+30.2	+37.4	+7.2	+0.81	+37.3	+46.8	+9.5	+0.80
2.E+08	17:12:23	+97	+30.0	+36.9	+6.9	+0.81	+37.3	+46.5	+9.2	+0.80
2.E+08	17:13:25	+99	+29.8	+36.6	+6.8	+0.81	+36.3	+45.4	+9.1	+0.80
3.E+08	17:14:26	+97	+29.5	+35.9	+6.4	+0.82	+36.7	+45.6	+8.9	+0.80
3.E+08	17:15:27	+97	+29.3	+35.6	+6.2	+0.82	+36.3	+44.8	+8.4	+0.81
3.E+08	17:16:29	+94	+29.1	+35.5	+6.3	+0.82	+36.0	+44.9	+8.7	+0.81
4.E+08	17:17:30	+94	+29.0	+35.2	+6.1	+0.83	+35.7	+44.0	+8.3	+0.81
4.E+08	17:18:32	+95	+29.1	+35.3	+6.1	+0.83	+35.6	+43.9	+8.3	+0.81
4.E+08	17:19:33	+95	+28.9	+35.1	+6.1	+0.83	+35.4	+43.7	+8.3	+0.81
5.E+08	17:20:35	+96	+28.3	+34.4	+6.1	+0.82	+35.1	+43.3	+8.2	+0.81
5.E+08	17:21:37	+96	+28.4	+34.3	+5.9	+0.83	+34.8	+42.8	+8.1	+0.81
5.E+08	17:22:38	+99	+28.2	+33.9	+5.8	+0.83	+34.9	+42.7	+7.8	+0.82
5.E+08	17:23:40	+97	+28.5	+33.8	+5.4	+0.84	+34.8	+42.8	+8.1	+0.81
6.E+08	17:24:41	+95	+28.4	+34.0	+5.7	+0.83	+34.1	+42.1	+8.0	+0.81
6.E+08	17:25:43	+95	+27.8	+33.6	+5.8	+0.83	+34.6	+42.5	+7.9	+0.81
6.E+08	17:26:44	+97	+27.9	+33.5	+5.7	+0.83	+34.5	+42.3	+7.8	+0.82
6.E+08	17:27:46	+96	+27.7	+33.3	+5.6	+0.83	+34.7	+42.3	+7.6	+0.82
7.E+08	17:28:47	+97	+27.9	+33.5	+5.6	+0.83	+34.3	+42.1	+7.8	+0.82
7.E+08	17:29:49	+97	+27.6	+33.1	+5.5	+0.83	+34.2	+42.4	+8.1	+0.81

Probe 0 :\MBYTE\DAT\F6119RR3.IO
Probe 0 :\MBYTE\DAT\F6119RR5.DO
Probe 1 :\MBYTE\DAT\F6119L8.IO
Probe 1 :\MBYTE\DAT\F6119L8.DO

8.E+08	17:30:51	+98	+27.6	+33.0	+5.4	+0.84	+34.0	+41.7	+7.7	+0.82
8.E+08	17:31:52	+95	+27.3	+32.7	+5.4	+0.84	+33.7	+41.6	+7.9	+0.81
8.E+08	17:32:54	+96	+27.3	+32.7	+5.4	+0.84	+33.9	+41.1	+7.2	+0.33
8.E+08	17:33:55	+97	+27.3	+32.3	+5.0	+0.85	+34.1	+41.5	+7.4	-0.32
9.E+08	17:34:57	+98	+27.5	+32.6	+5.3	+0.84	+34.0	+41.6	+7.6	+0.82
9.E+08	17:35:58	+98	+26.8	+32.1	+5.3	+0.84	+33.5	+41.0	+7.5	+0.82
9.E+08	17:37:00	+95	+26.9	+32.2	+5.3	+0.84	+33.4	+40.9	+7.6	+0.81
1.E+09	17:38:01	+97	+26.9	+32.0	+5.1	+0.84	+33.6	+41.0	+7.4	+0.82
1.E+09	17:39:03	+94	+26.9	+31.9	+5.0	+0.84	+33.5	+40.9	+7.5	+0.52

Forward Voltage = 5.917155 volts Reverse Voltage = -5.979818 volts

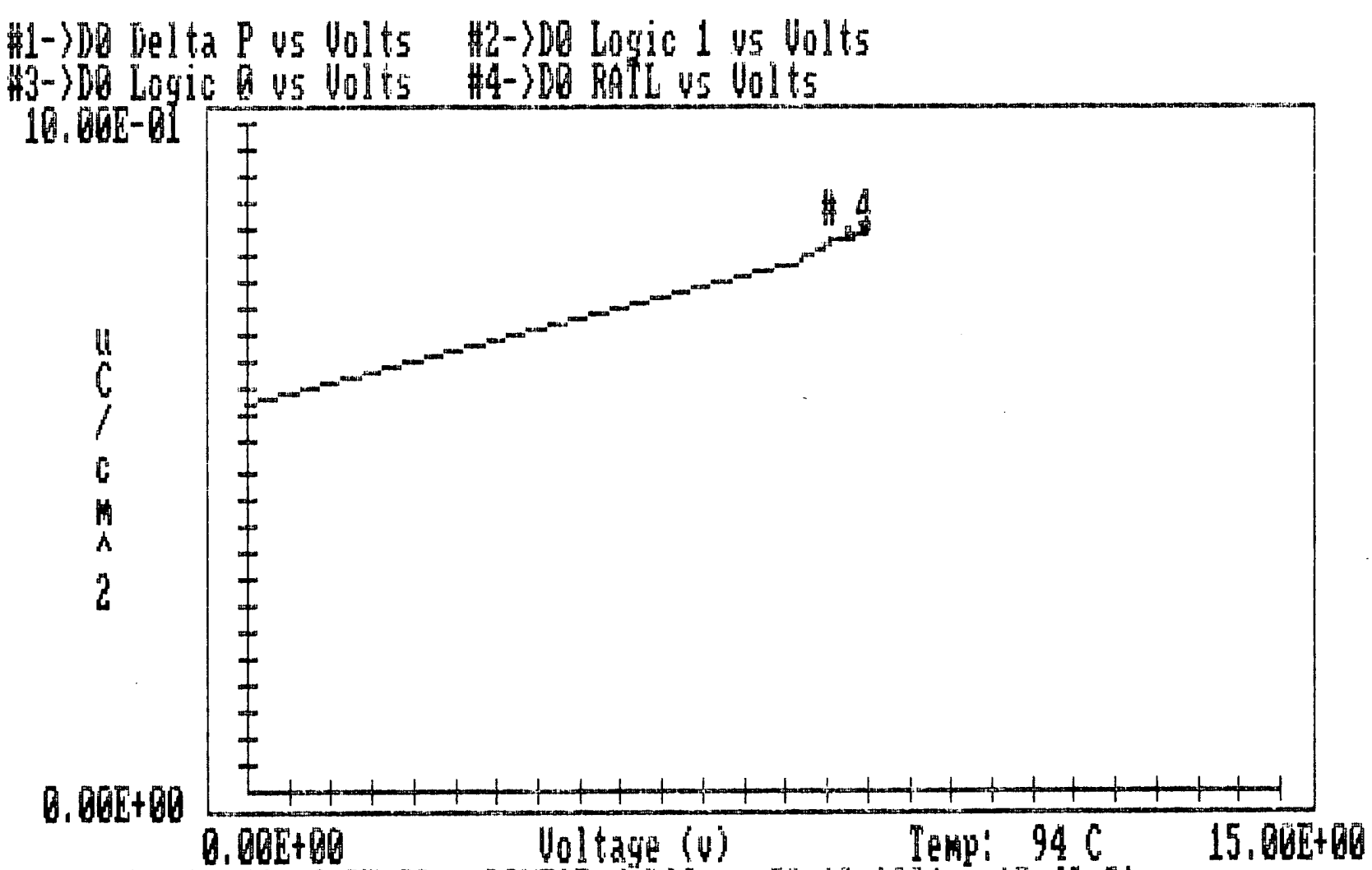
#1->D0 Delta P vs Volts #2->D0 Logic 1 vs Volts
#3->D0 Logic 0 vs Volts #4->D0 RATL vs Volts



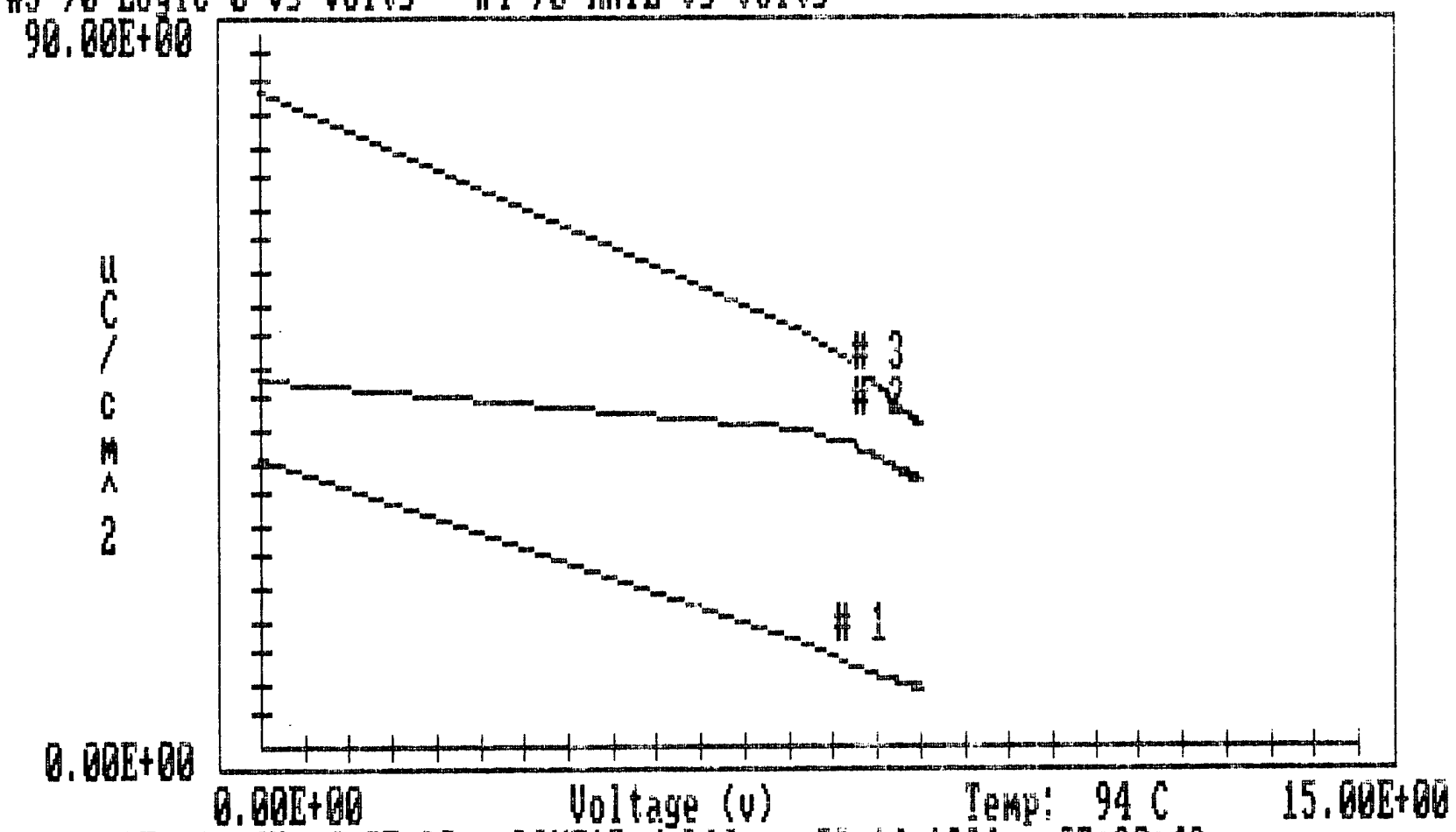
Temp: 94 C

dX= 6.0E-01 dY= 3.0E+00 LINEAR / LOG 08-13-1986 17:41:44

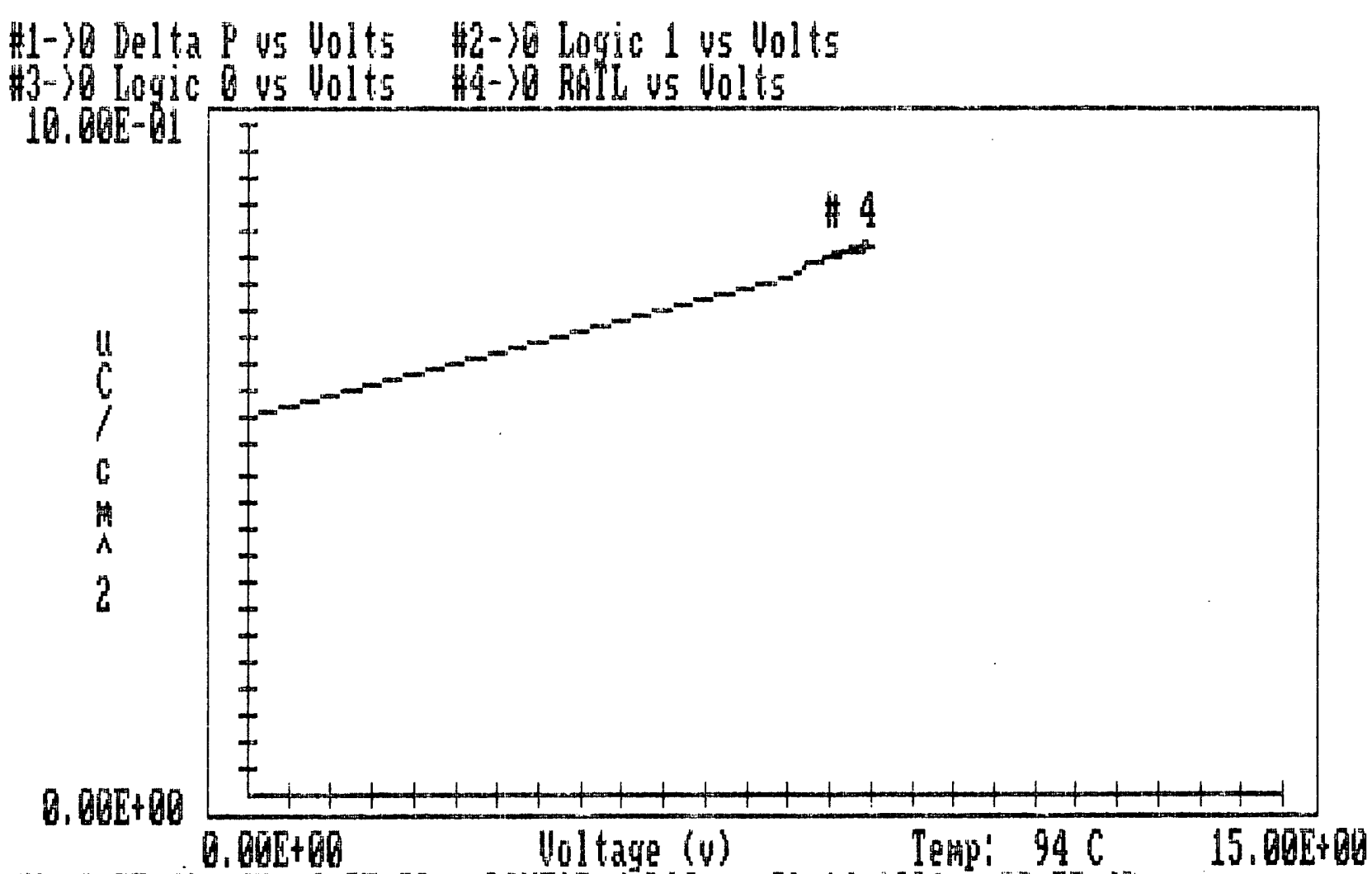
Datafile = \MBYTE\DAT\F6119RR5.D0
Comp = 3/40/60 W/10 Thick = .5 microns 08-13-1986 17:39:28
Mode = PULSE Trigger time = .00002 secs Freq = 750000 Hz



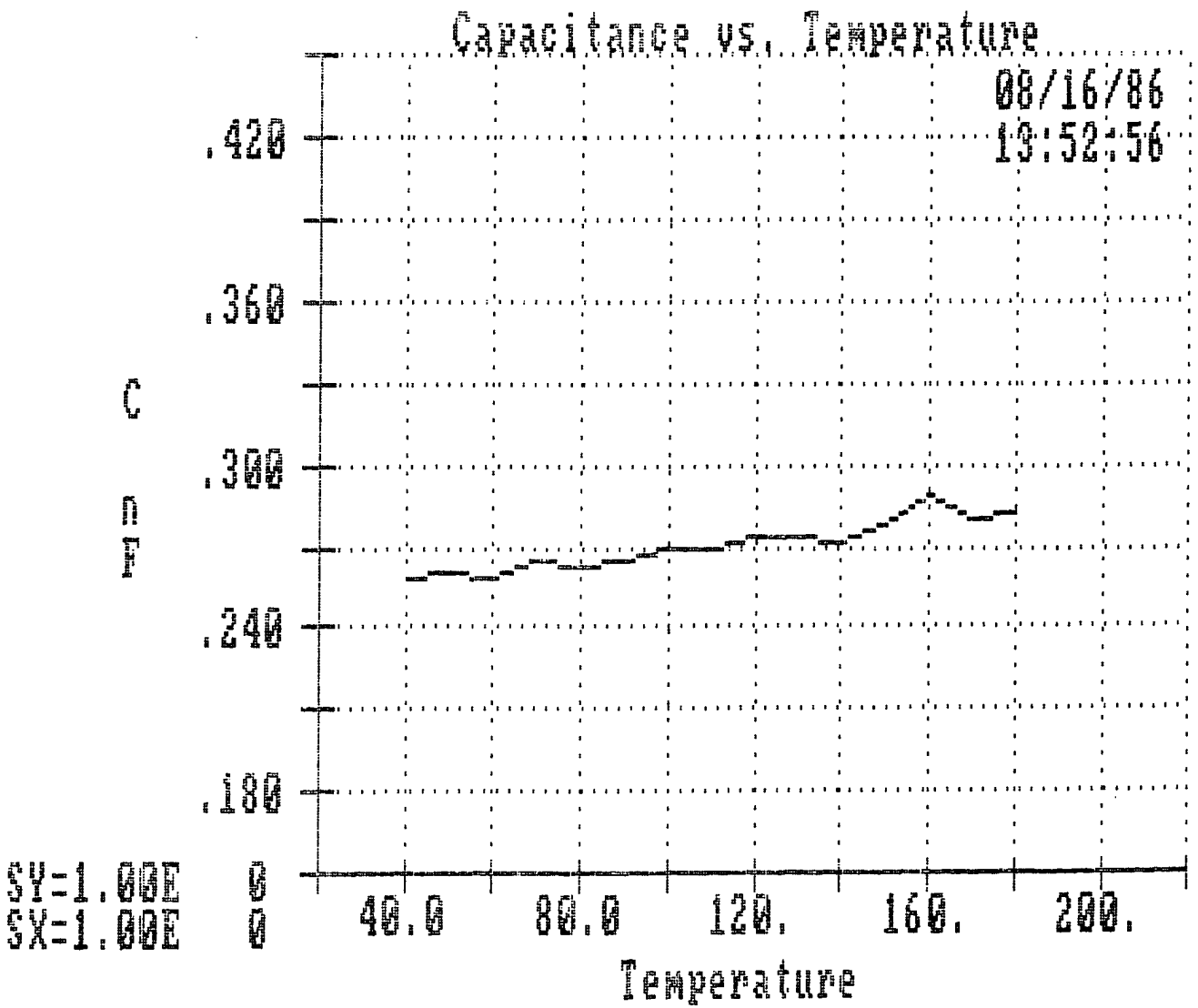
Datafile = \MBYTE\DAT\F6119RR5.D0
Comp = 3/40/60 W/10 Thick = .5 microns 08-13-1986 17:39:28
Mode = PULSE Trigger time = .00002 secs Freq = 750000 Hz



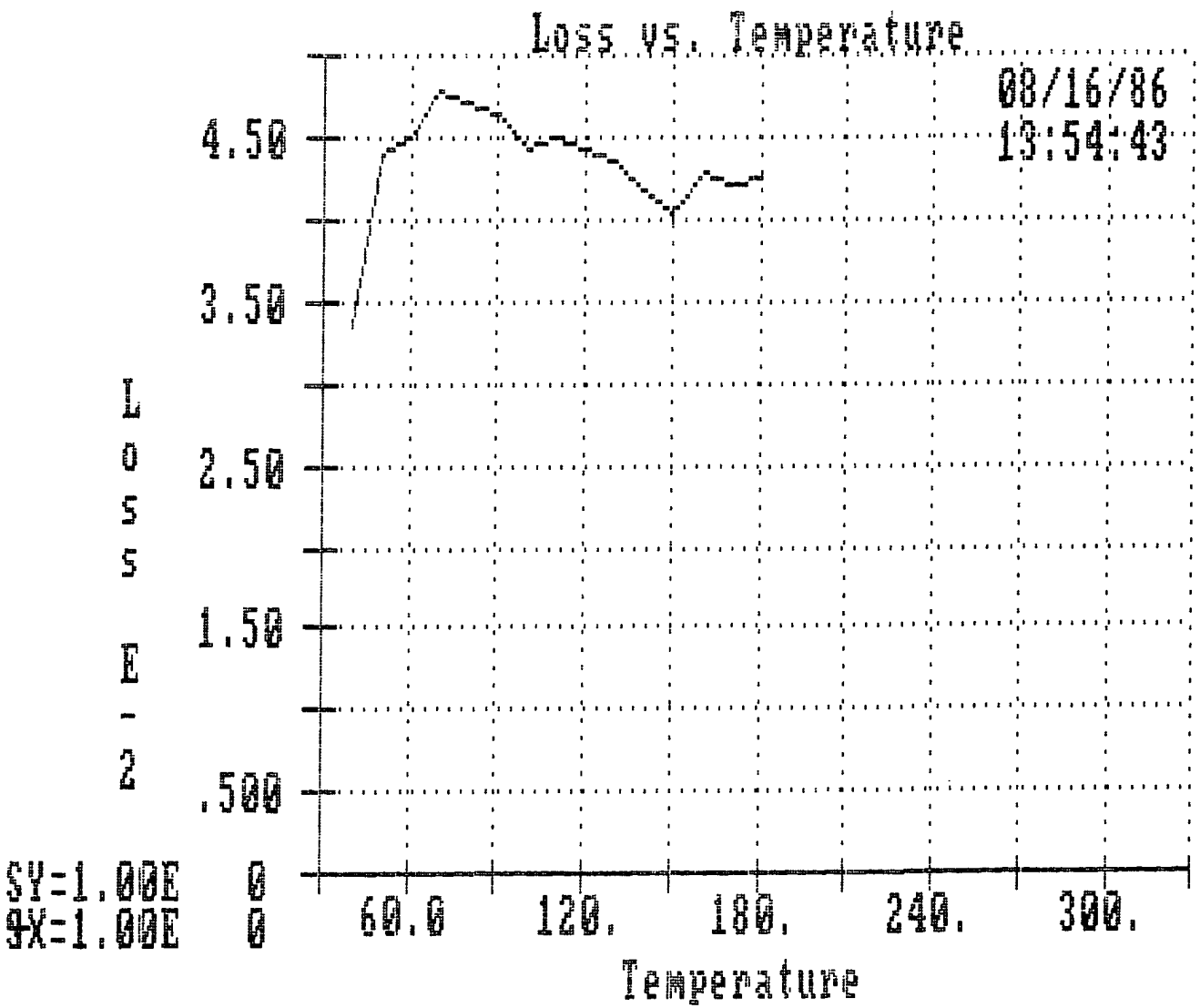
Datafile = \MBYTE\DAT\F6119L8.D0
Comp = 3/40/60 W/10 Thick = .5 microns 08-13-1986 17:39:45
Mode = PULSE Trigger time = .00002 secs Freq = 750000 Hz


#1->0 Delta P vs Volts
#2->0 Logic 1 vs Volts
#3->0 Logic 0 vs Volts
#4->0 RAIL vs Volts
10.00E-01
4
u C / c M ^ 2
0.00E+00
0.00E+00
Voltage (v)
Temp: 94 C
15.00E+00
dX= 6.0E-01 dY= 4.0E-02 LINEAR / LOG 08-14-1986 07:55:45
Datafile = \MBYTE\DAT\F6119L8.D0
Comp = 3/40/60 W/10 Thick = .5 microns 08-13-1986 17:39:45
Mode = PULSE Trigger time = .00002 secs Freq = 750000 Hz

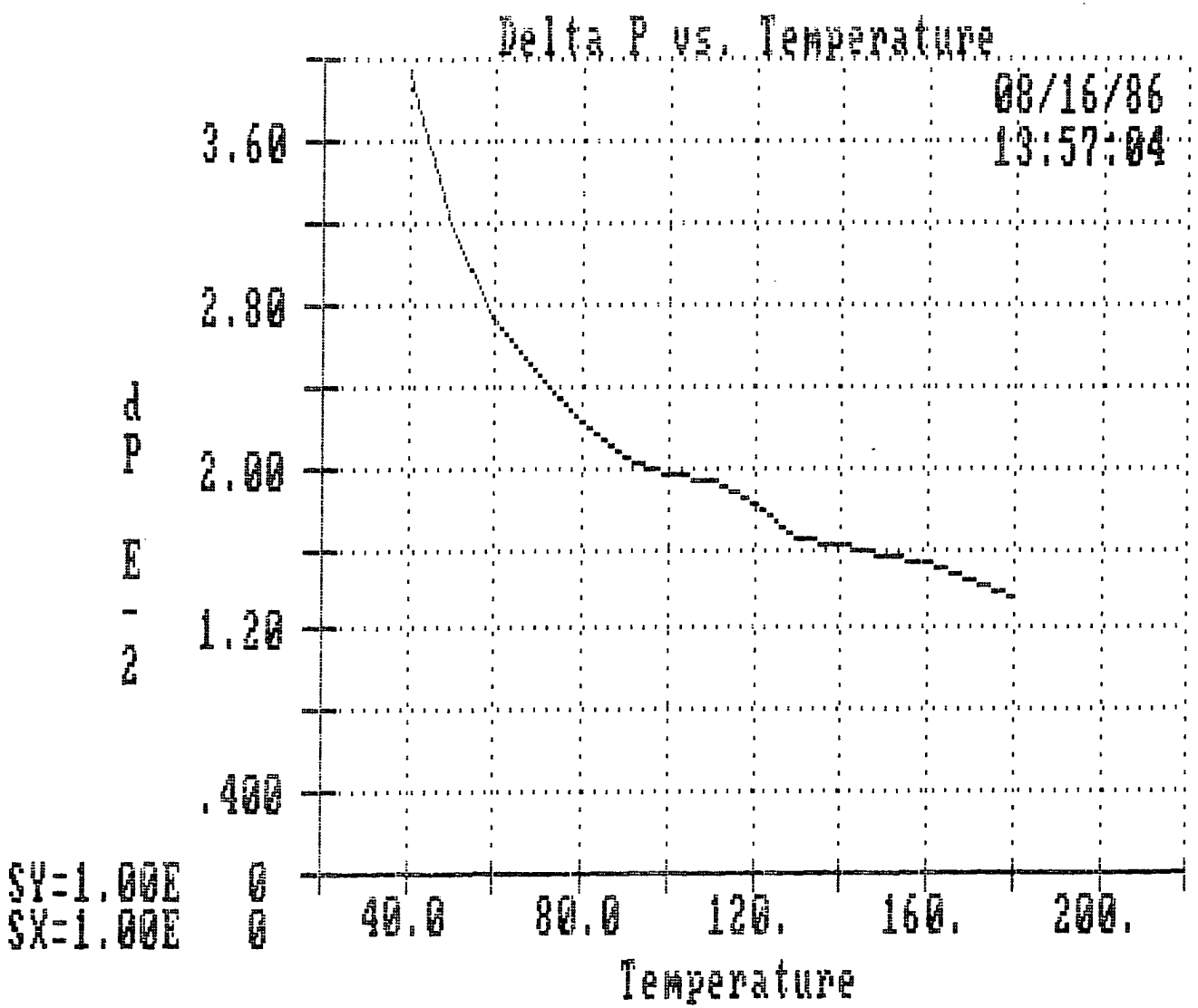
FLOG 6119
CELL R3
CURIE_



FLOG 6119
CELL R3
CURIE_



FLOG 6119
CELL R3_



Wafers from foundary after CONT

1. LPCVD Nitride
   * contact ox
   * 0.2u silicon nitride

2. Sputter BEL
   * Ti or TixNy ~50nm
   * Pt ~ 0.2u

3. Pattern BEL

4. BEL etch
   * stop on either SixNy or TixNy

5. Deposit ferroelectric

6. Deposit TEL

7. Pattern TEL

8. Etch TEL

9. Pattern FES

10. Etch FES

11. Pattern SIN

12. Etch SixNy (can also remove any remaining TixOy)

13. Remove oxide from contacts

14. Deposit Al

15. Pattern METAL

16. Etch Al

17. Alloy

18. Deposit passivation

19. Pattern PO

20. Etch passivation

Critical Dimensions

Layer	Mask	Resist	Final
BEL	10.5+-0.25	10.0+-0.5	9.0+-0.5
TEL	10.5+-0.25	10.0+-0.5	9.0+-

ORBIT SEMICONDUCTOR, INC.
A SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

ORDER ACKNOWLEDGEMENT

4

DATE	PAGE
~~9/18/86~~	1

SOLD TO 1004000 C002331

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

TERMS	PURCHASE ORDER NO.	SALES NO.	ORDER DATE	REQUEST DATE	SHIP VIA
O.D	0986011	0	9/17/86	9/17/86	FED EXP P1

	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY		PRICE
	1	140020-CIF	TAPE CONVERSION	LT		1	900.00
	1	140020-CONV	DATA SIZING & CONVERSION	LT		1	1,600.00
	1	540400-PLOTS	VERSATEC PLOTS	EA	975	13	975.00
	1	140001-3SCMOS-N	3U SINGLE POLY CMOS-N CHANNEL PART NAME: TD01 . ONE WAFER COMPLETELY PROCESSED, BALANCED TO BE SHIPPED THROUGH CONTACT ETCH W/ ADDITIONAL NITRIDE.OXIDE FILM.	LT		1	12,150.00
	1	140002-TEST	TEST WAFERS BARE SILICON W/ FLO GLASS LAYER DEPOSITED W/ CONTACT MASK LEVEL ETCHED IN, AND REOXIDATION OF CONTACT OPENINGS AND SILICON NITRIDE DEPOSITIO	EA	4925	25	197.00

ORIGINAL

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TELEPHONE (408) 744-1800
TWX (910) 339-9307

ORDER ACKNOWLEDGEMENT

DATE	PAGE
9/18/86	2

SOLD TO 1004000 C002331

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

TERMS	PURCHASE ORDER NO.	SALES NO.	ORDER DATE	REQUEST DATE	SHIP VIA
O.D	0986011	0	9/17/86	9/17/86	FED EXP P1

	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY	PRICE
1		140020-MASK	MASK GENERATION SODA LIME GLASS - 13 LAYERS 5" X 5" FOR CONTACT PRINTING TOTAL LINE ITEMS 6	✓CT	18.200 13	1,400.00 38750.00

ORIGINAL

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1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

INVOICE	PAGE
8208	1
DATE	
9/30/86	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FED EXP P1	C002331		0986011	PREPAY & C.O.D.

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
140020-CIF	TAPE CONVERSION	LT	1		900.000	900.00
140020-CONV	DATA SIZING & CONVERSION	LT	1		1,600.000	1,600.00
540400-PLOTS	VERSATEC PLOTS	EA	13		75.000	975.00
140001-3SCMOS-N	3U SINGLE POLY CMOS-N CHANNEL PART NAME: TD01 . ONE WAFER COMPLETELY PROCESSED, BALANCED TO BE SHIPPED THROUGH CONTACT ETCH W/ ADDITIONAL NITRIDE.OXIDE FILM.	LT		1	12,150.000	
140002-TEST	TEST WAFERS BARE SILICON W/ FLO GLASS LAYER DEPOSITED W/ CONTACT MASK LEVEL ETCHED IN, AND REOXIDATION OF CONTACT OPENINGS AND SILICON NITRIDE DEPOSITIO	EA		25	197.000	
140020-MASK	MASK GENERATION SODA LIME GLASS - 13	LT	13		1,400.000	18,200.00

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
						CONTINUED

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

8208	2
DATE	
9/30/86	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FED EXP P1	C002331		0986011	PREPAY & C.O.D.

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
	LAYERS 5" X 5" FOR CONTACT PRINTING . . THANK YOU FOR YOUR PAYMNT					

9-18-86
Wire transfer
$ 21,675.00
715512

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	21,675.00					21,675.00

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

ORDER ACKNOWLEDGEMENT

DATE	PAGE
1/15/87	1

SOLD TO 1- 1004000 C002423

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

TERMS	PURCHASE ORDER NO.	SALES NO.	ORDER DATE	REQUEST DATE	SHIP VIA
C.O.D	0187007	4	1/15/87	1/15/87	FED EXP P1

REL. NO.	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY	PRICE
	1	140020-PLT	VERSATEC PLOTS	EA	3	75.000
	1	140020-MASK	MASK GENERATION 5 X 5 SODA LIME GLASS	LT	3	1,400.000
	1	540400-CONV	DATA CONVERSION	LT	1	600.000
			TOTAL LINE ITEMS 3			

5

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

PACKING SLIP

SHIP TO:

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE
NM 87109

SOLD TO:

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE
NM 87109

DATE	PAGE
1/22/87	1
PURCHASE ORDER NO.	SALES ORDER NO.
0187007	C002423

SHIPPING INSTRUCTIONS

fedexp # 150879141

FED EXP P1

SHIPPED BY	NO. OF PKGS.	TOTAL WEIGHT
BY	1	4 lbs

ITEM NUMBER	DESCRIPTION	QUANTITY ORDERED	U/M	QUANTITY SHIPPED	U/M	QTY BACK ORDERED	U/M
140020-MASK	MASK GENERATION 5 X 5 SODA LIME GLASS	3	LT	3	lt	at 75.00	225.00
140020-PLT	VERSATEC PLOTS	3	EA	3	lt	at 1400.00	4200.00
540400-CONV	DATA CONVERSION	1	LT	1	lt	at 830.00	830.00
							5255.00

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
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1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

ORDER ACKNOWLEDGEMENT

DATE	PAGE
3/06/87	1

1- 1004000 C002490

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

TERMS	PURCHASE ORDER NO.	SALES NO.	ORDER DATE	REQUEST DATE	SHIP VIA
C.O.D	0387009	4	3/05/87	3/05/87	FED EXP P1

REL. NO.	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY	PRICE
			PRODUCT NAME: ECD512			
	1	540400-CONV	DATA CONVERSION	LT	1	900.000
	1	140020-PLT	VERSATEC PLOTS BLOWBACK FILMS	EA	14	75.000
	1	140020-MASK	MASK GENERATION LOW EXPANSION GLASS PLATES	LT	16	1,200.000
	1	140001-3SCMOS-N	3U SINGLE POLY CMOS-N WELL . ONE WAFER COMPLETELY PROCESSED, BALANCE TO BE SHIPPED THRU CONTACT ETCH GROW 250ANGS +/- 25ANGS DEPOSIT NITRIDE 350ANGS	LT	1	12,150.000
	1	140002-TEST	TEST WAFERS 1. DEPOSIT LTO TO OUR STD THICKNESS. 2. CONTACT MASK & ETCH	EA	25	119.000

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

DATE	PAGE
3/06/87	2

1- 1004000 C002490

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

TERMS	PURCHASE ORDER NO.	SALES NO.	ORDER DATE	REQUEST DATE	SHIP VIA
C.O.D	0387009	4	3/05/87	3/05/87	FED EXP P1

REL. NO.	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY	PRICE
			3. DENSIFY 4. CONTACT REOXIDATION TO 250 DEG ANGSTROMS. 5. DEPOSIT LPCVD NITRIDE TO 750 DEG ANGSTROMS TOTAL LINE ITEMS 5			

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION
1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

SHIPPING AUTHORIZATION ☒

DEBIT MEMO ☐

SHIP TO: Krysalis
3825 Academy Parkway So.
N.E. Albuquerque, N.M.
87109

S/A NO. 01009

DM NO. _____

DATE: 4-14-87

ITEM	QUANTITY	UNIT	DESCRIPTION	AMOUNT UNIT	AMOUNT EXT.
1	1	EA	ECD512 Lot # 03M13A (1) Wafer	N/C	—

PO # 0387009
SO # 2490
Inv. date: 4/12/87

TO BE COMPLETED BY ORIGINATOR

REASON FOR SHIPMENT

- ☒ PREPAID →
- ☐ WORK ON P.O. _____
- ☐
- ☐ SURPLUS SALE
- ☐ ADVERTISING LITERATURE
- ☐ PURCHASE RETURN
- ☐ OTHER _____

INVOICE NO. * _____

REASON _____

- ☐ CREDIT ONLY
- ☐ REPLACEMENT

TO BE COMPLETED BY PURCHASING OR SALES

F.O.B.	CHARGES	INSURED
☐ ORBIT, SUNNYVALE	☐ PREPAID	☐ YES ☐ NO
☐ DESTINATION	☐ COLLECT	VALUE $ _____

SHIP VIA

- ☐ WILL CALL *
- ☐ UPS
- ☐ PARCEL POST
- ☐ 1ST CLASS MAIL
- ☐ COMMON CARRIER
- ☐ AIR MAIL
- ☐ AIR FREIGHT
- ☐ ORBIT TRUCK *
- ☐ OTHER
- ☐ FED EX 331886526

(SPECIFY) _____

ORIGINATOR'S NAME	EXT.	VENDOR'S RETURN AUTHORIZATION BY
DEPT.		SIGNATURE (PURCH. OR SALES) EXT.

TO BE COMPLETED BY SHIPPING

DATE SHIPPED	B/L NO.	NO. PCS.	WEIGHT	PREPAID CHARGE	SHIPPING SIGNATURE	RECEIVED BY *

PACKING SHEET

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

8816	1
DATE	
3/24/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FED EXP P1	C002490	4	0387009	PREPAY MASKS& NET 10

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
	PRODUCT NAME: ECD512					
540400-CONV	DATA CONVERSION	LT	1		900.000	900.00
540400-CONV	DATA CONVERSION	LT	1		1,000.000	1,000.00
	ADDITIONAL DATA CONV.					
	COSTS FOR 5 LAYERS					
140020-PLT	VERSATEC PLOTS	EA	14		75.000	1,050.00
	BLOWBACK FILMS					
140020-MASK	MASK GENERATION	LT	5		350.000	1,750.00
	PG COSTS					
	FOR RETICLES FOR 5 LAYERS					
140020-MASK	MASK GENERATION	LT	16		1,200.000	19,200.00
	LOW EXPANSION GLASS					
	PLATES					
140001-3SCMOS-N	3U SINGLE POLY CMOS-N WELL	LT		1	12,150.000	
	ONE WAFER COMPLETELY					
	PROCESSED, BALANCE TO BE					
	SHIPPED THRU CONTACT ETCH					
	GROW 250ANGS +/- 25ANGS					
	DEPOSIT NITRIDE 350ANGS					
	Thank you for your 3/13/87 payment of $21,150.00 (Check #2395)				Balance Due	2,750.00

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS	TAXES	TERMS DISCOUNT	AMOUNT DUE
	23,900.00					23,900.00

REC'D March 30, 87
APPROVED
VENDOR # CA23
GL ACCT # 7160.12
DATE PAID 4-30-87
CK # ORIGINAL 2688

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

8886	1
DATE	
4/03/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FED EXP P1	C002490	4	0387009	PREPAY MASKS& NET 10

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
140001-3SCMOS-N	PRODUCT NAME: ECD512 3U SINGLE POLY CMOS-N WELL . ONE WAFER COMPLETELY PROCESSED, BALANCE TO BE SHIPPED THRU CONTACT ETCH GROW 250ANGS +/- 25ANGS DEPOSIT NITRIDE 350ANGS	LT		1	12,150.000	
140002-TEST	TEST WAFERS 1. DEPOSIT LTO TO OUR STD THICKNESS. 2. CONTACT MASK & ETCH 3. DENSIFY 4. CONTACT REOXIDATION TO 250 DEG ANGSTROMS. 5. DEPOSIT LPCVD NITRIDE TO 750 DEG ANGSTROMS	EA	25		119.000	2,975.00
	FED-X P1 OVERNIGHT LETTER					9.53

RSC'D April 13, 87
APPROVED
VENDOR #: CA73
GL ACCT #: 7160.11
DATE PAID: 4-30-87
CK #: 2648

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	2,975.00		9.53			2,984.53

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

PACKING SLIP

SHIP TO:

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE
NM 87109

SOLD TO:

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE
NM 87109

DATE	PAGE
4-12-87	1
PURCHASE ORDER NO.	SALES ORDER NO.
0387009	C002490
SHIPPING INSTRUCTIONS	
FED EXP P1 331-8865-432	
SHIPPED BY	NO. OF PKGS. / TOTAL WEIGHT
[illegible]	1 / 3#

ITEM NUMBER	DESCRIPTION	QUANTITY ORDERED	U/M	QUANTITY SHIPPED	U/M	QTY BACK ORDERED	U/M
	PRODUCT NAME: ECD512						
140001-3SCM03U	SINGLE POLY CMOS-N WELL ONE WAFER COMPLETELY PROCESSED, BALANCE TO BE SHIPPED THRU CONTACT ETCH GROW 250ANGS +/- 25ANGS DEPOSIT NITRIDE 350ANGS ECD512 03M113 (7)	1	LT	1	LT	Ø	

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
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1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

INVOICE	PAGE
8916	1
DATE	
4/13/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FED EXP P1	C002490	4	0387009	PREPAY MASKS& NET 10

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
140001-3SCMOS-N	PRODUCT NAME: ECD512 B 3U SINGLE POLY CMOS-N WELL • ONE WAFER COMPLETELY PROCESSED, BALANCE TO BE SHIPPED THRU CONTACT ETCH GROW 250ANGS +/- 25ANGS DEPOSIT NITRIDE 350ANGS FED-X P1 331 8865 432 B - ITEM PREVIOUSLY BACKORDERED	LT	1		8,505.000	8,505.00 20.00

REC'D April 17, 87
APPROVED
VENDOR # CA23
GL ACCT # 7160.11
DATE PAID 4-30-87
CK # 2648

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	8,505.00		20.00			8,525.00

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

ORDER ACKNOWLEDGEMENT

DATE 4/27/87

PAGE 1

1- 1004000 C002558

SOLD KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

C.O. ITEMS	PURCHASE ORDER NO.	SALES NO. 4	ORDER DATE 4/27/87	REQUESTED 5/19/87	FEDERAL EXPRESS SHIP VIA
	048T054				

REL. NO.	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY	PRICE
	1	140004-3SCMOS-N	3U S/P CMOS - N WELL - PROD PROCESS 1 WAFER COMPLE. W/ THE BALANCE TO BE PROCESSED THR. CONTACT MASK, ETCH AND CLEAN, GROW 250A +- 25A DEPOSIT NITRIDE 750A+-50A TOTAL LINE ITEMS 1	EA	25	967.000

REC'D May 1, 87
APPROVED
VENDOR # CA23
GL ACCT #

DATE PAID 6-19-87
CK # 1033

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

PACKING SLIP

SHIP TO:

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE
NM 87109

SOLD TO:

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE
NM 87109

DATE	PAGE
5-21-87	1
PURCHASE ORDER NO.	SALES ORDER NO.
0487054	C002558
SHIPPING INSTRUCTIONS	
FEDERAL EXPRESS P1 3318865353	

SHIPPED BY	NO. OF PKGS.	TOTAL WEIGHT
Fedex	1	

ITEM NUMBER	DESCRIPTION	QUANTITY ORDERED	U/M	QUANTITY SHIPPED	U/M	QTY BACK ORDERED	U/M
140004-3SCMO	3U S/P CMOS - N WELL - PROD PROCESS 1 WAFER COMPLE. W/ THE BALANCE TO BE PROCESSED THR. CONTACT MASK, ETCH AND CLEAN, GROW 250A +- 25A OXIDE DEPOSIT NITRIDE 750A+-50A	25	EA	19		6	

04M129 (18) on hold after Nitride dep of 743 A ....

04M129A (1) completed

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

INVOICE	PAGE
9081	1
DATE	
5/21/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FEDERAL EXPRESS P1	C002558	4	0487054	C.O.D

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
140004-3SCMOS-N	3U S/P CMOS - N WELL - PROD PROCESS 1 WAFER COMPLE. W/ THE BALANCE TO BE PROCESSED THR. CONTACT MASK, ETCH AND CLEAN, GROW 250A +- 25A DEPOSIT NITRIDE 750A+-50A	EA	19	6	967.000	18,373.00
	FED-X P1 331 8868 383					20.00

REC'D May 27, 87
APPROVED
VENDOR # CA23
GL ACCT #
DATE PAID
CK #

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	18,373.00		20.00			18,393.00

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

INVOICE	PAGE
8977	1
DATE	
4/30/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FEDERAL EXPRESS P1	C002555	4	0487044	C.O.D

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
540400-CONV	DATA CONVERSION	LT	1		900.000	900.00
140020-PLT	VERSATEC PLOTS	EA	2		75.000	150.00
540400-CONV	DATA CONVERSION	LT	2		350.000	700.00
140020-MASK	MASK GENERATION	LT	2		1,200.000	2,400.00

REC'D May 5, 87
APPROVED
VENDOR # CA23
GL ACCT # 7155.12
DATE PAID 5/28/87
CK # 2729

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	4,150.00					4,150.00

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

PACKING SLIP

SHIP TO:

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE
NM 87109

SOLD TO:

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE
NM 87109

DATE	PAGE
4-30-87	1
PURCHASE ORDER NO.	SALES ORDER NO.
0487044	C002555
SHIPPING INSTRUCTIONS	
3318865922 FEDERAL EXPRESS P1	
SHIPPED BY	NO. OF PKGS. / TOTAL WEIGHT
B FOD6	2

ITEM NUMBER	DESCRIPTION	QUANTITY ORDERED	U/M	QUANTITY SHIPPED	U/M	QTY BACK ORDERED	U/M
540400-CONV	DATA CONVERSION	1	LT	1	LT	ϕ	
140020-PLT	VERSATEC PLOTS	2	EA	2	EA	ϕ	
540400-CONV	DATA CONVERSION (RETICLES)	2	LT	2	LT	ϕ	
140020-MASK	MASK GENERATION	2	LT	2	LT	ϕ	

ORBIT SEMICONDUCTOR, INC.
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SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

INVOICE	PAGE
9069	1
DATE	
5/19/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FEDERAL EXPRESS P1	C002595	4	0587013	C.O.D

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
540400-CONV	DATA CONVERSION	LT	1		900.000	900.00
140020-PLT	VERSATEC PLOTS BLOWBACK FILMS	EA	1		75.000	75.00
540400-CONV	DATA CONVERSION RETICLES	LT	1		350.000	350.00
140020-MASK	MASK GENERATION LOW EXPANSION GLASS PLATES	LT	1		1,200.000	1,200.00
	FED-X P1 331 8866 795					21.89

REC'D May 27, 87
APPROVED
VENDOR # CA23
GL ACCT # 7160.12
DATE PAID 6-19-87
CK # 1033

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	2,525.00		21.89			2,546.89

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

ORDER ACKNOWLEDGEMENT

DATE	PAGE
6/05/87	1

1- 1004000 C002616

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

TERMS	PURCHASE ORDER NO.	SALES NO.	ORDER DATE	REQUEST DATE	SHIP VIA
C.O.D	0687010	4	6/05/87	6/05/87	FEDERAL EXPRESS P1

REL. NO.	LOCATION	ITEM NUMBER	DESCRIPTION	U/M	ORDER QUANTITY	PRICE
	1	540400-CONV	DATA CONVERSION	LT	1	900.000
	1	140020-PLT	VERSATEC PLOTS	EA	3	75.000
	1	540400-CONV	DATA CONVERSION RETICLES	LT	3	350.000
	1	140020-MASK	MASK GENERATION	LT	3	1,200.000
			TOTAL LINE ITEMS 4			

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

INVOICE

INVOICE	PAGE
9173	1
DATE	
6/15/87	

SOLD TO
KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE NM 87109

SHIP TO
KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE NM 87109

CUST. NO.	SHIP VIA	ORDER NO.	SLS. NO.	PURCHASE ORDER	TERMS
1- 1004000	FEDERAL EXPRESS P1	C002616	4	0687010	C.O.D

ITEM NUMBER	DESCRIPTION	U/M	QUANTITY SHIPPED	QUANTITY BACK ORDERED	UNIT PRICE	AMOUNT
540400-CONV	DATA CONVERSION	LT	1		900.000	900.00
140020-PLT	VERSATEC PLOTS	EA	3		75.000	225.00
540400-CONV	DATA CONVERSION RETICLES	LT	3		350.000	1,050.00
140020-MASK	MASK GENERATION	LT	3		1,200.000	3,600.00

REC'D June 19, 87
APPROVED
VENDOR # CA23
GL ACCT # 7155.12
DATE PAID 7-31-87
CK # 1261

TOTAL WEIGHT	NET SALES AMOUNT	TRADE DISCOUNT	MISCELLANEOUS CHGS.	TAXES	TERMS DISCOUNT	AMOUNT DUE
	5,775.00					5,775.00

ORIGINAL

ORBIT SEMICONDUCTOR, INC.
SUBSIDIARY OF ORBIT INSTRUMENT CORPORATION

1230 BORDEAUX DRIVE
SUNNYVALE, CALIFORNIA 94089-1277
TELEPHONE (408) 744-1800
TWX (910) 339-9307

PACKING SLIP

SHIP TO:

KRYSALIS
3825 ACADEMY PARKWAY,
SOUTH, N.E.
ALBUQUERQUE
NM 87109

SOLD TO:

KRYSALIS
4200 OSUNA N.E. #102
BOX 106
ALBUQUERQUE
NM 87109

DATE	PAGE
6-15-87	1
PURCHASE ORDER NO.	SALES ORDER NO.
0687010	C002616

SHIPPING INSTRUCTIONS

3318867752
FEDERAL EXPRESS P1

SHIPPED BY	NO. OF PKGS.	TOTAL WEIGHT
	1	3

ITEM NUMBER	DESCRIPTION	QUANTITY ORDERED	U/M	QUANTITY SHIPPED	U/M	QTY BACK ORDERED	U/M
540400-CONV	DATA CONVERSION	1	LT	1	LT	0	
140020-PLT	VERSATEC PLOTS	3	EA	3	EA		
540400-CONV	DATA CONVERSION RETICLES	3	LT	3	LT		
140020-MASK	MASK GENERATION	3	LT	3	LT		

SHIPPED
APR 02 1987

INDY ELECTRONICS, INC.

INDY ELECTRONICS, INC.
Telephone (209) 239-4444
TLX 359445 Indyelec Mntc
TWX 5107651004 Indyelec Mntc
Post Office Box 2301
400 Industrial Park Drive
Manteca, California 95336

PACKING LIST

№ 46190

6

SOLD TO
KRYSALIS CORPORATION
3825 ACADEMY PARKWAY SOUTH NE
ALBEQUERQUE, NM 87109
ATTN: MICHAEL CORDOBA

SHIP TO
SAME

DATE SHIPPED	INDY P.O. NUMBER	CUSTOMER P.O. NUMBER	CUSTOMER NAME	PARTIAL ☐
4/2/87	KCANM016S001A0-13054C	0387049	KRYSALIS CORP.	COMPLETE ☐
F.O.B.	SHIPPED VIA		NO. OF BOXES	WEIGHT
MANTECA	FEDERAL EXPRESS # 3991736840			

ITEM	QUANTITY	DESCRIPTION
1	2,666*	16 LEAD SIDEBRAZE DEVICE STRUCTURE 1

RUN #	W-LOT #	QTY
13054C-02AA-1	7076A	688*
03AA-1	~~7079~~ 7076B	602*
04AA-1	7069D	1376*

* EXCESS DIE RETURN TO CUSTOMER

White - Shipping Green - Traffic Canary - Accounting Pink - Material Control Gold - Production Control

Copy of Mother Lot

INDY STANDARD PCI - GOLD/TIN

CUSTOMER KRYSALIS CORP.

PKG TYPE/LEAD COUNT SIDEBRAZED/16

JOB ORDER # 13054C

MAINTAIN ANTISTATIC PRECAUTIONS

ASSEMBLY LOT # E2AA QTY 30

MAINTAIN WAFER LOT I. D.

INDY PART # KCANA016S-001A0

SHIP BY 4/9

CUSTOMER P/N STRUCTURE 1

DIE SIZE .082 X .056

DIE COUNT/CUST. 30

DIE I.D.#

DIE COUNT/INDY

WAFER LOT # 7076A

ORIGINATOR [signature] DATE 3/26/87 ENG [signature] DATE 3/26/87

REQUIRED MATERIAL:		DESCRIPTION:
PACKAGES	P/N CUSTOMER KIT	.180 X .140
D/A MAT'L	P/N 03-09-0045	84-1 LMI EPOXY ADHESIVE
WIRE	P/N 03-16-0022	(I) 1.25 MIL. AL (BLUE)
O/COAT MAT'L	P/N N/A	
LIDS	P/N 03-07-0006	.365 X .240 COMBO LID
H/SINK & EPOXY/SOLDER	P/N N/A P/N	
PKG/CARRIER LOAD MAT'L	P/N (I)	TUBES
INK	P/N 06-02-0003	MARKEM FRS-7224 WHITE EPOXY

SHIP VIA: FED-X

SPECIAL INSTRUCTIONS:

IF PRODUCT IS RECEIVED IN DIE FORM; N/A ALL DIE PREP PROCESS STEPS EXCEPT 2ND OPTICAL AND Q.A. GATE.

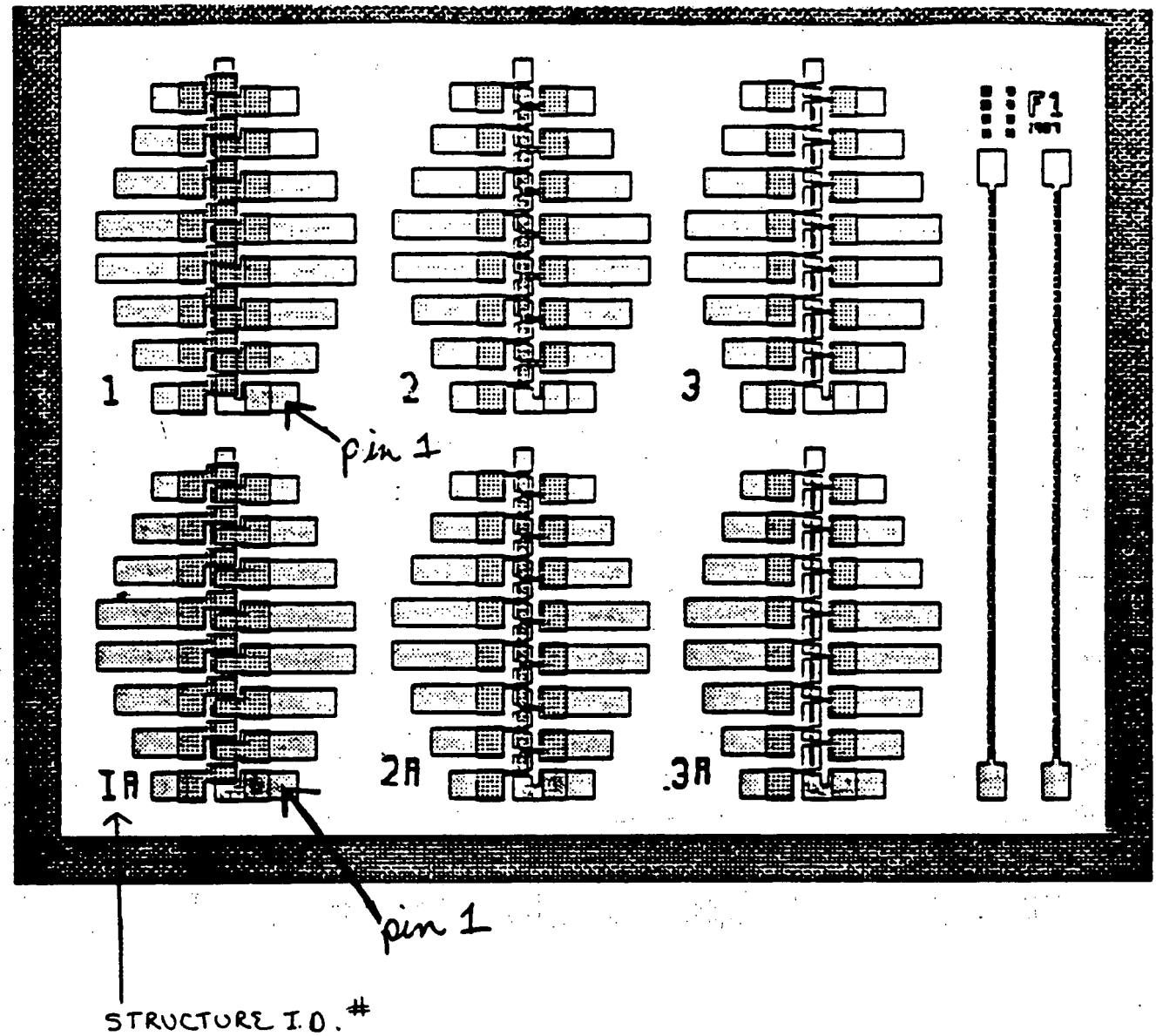
1. WAFER I.D. REQUIRED.
2. ** CAUTION ** DIE ARE UNGLASSIVATED - USE RUBBER TIPPED VACUUM PEN(s) ONLY.
3. WAFER SAW - CUT DIE STRUCTURES PER ATTACHED ILLUSTRATION(s).

INDY CONTROL # 20202767 REV N/C

I.D. # 13054C

SPECIAL INSTRUCTIONS (CONT.)

THE FIGURE BELOW DENOTES STRUCTURE I.D. NUMBER AND PIN 1 LOCATION.



OPERATION	QUANTITY IN	QUANTITY OUT	QUANTITY REJ	OPERATOR NUMBER	DATE	S	QA INSP	REMARKS	ENG OK
PRE WAFER WASH 0402-002 SPEC. INST.[X]	1/2	1/2		2442	3/27/87	1			N/A N/A
	EQUIPMENT# 395								
WAFER MOUNT 0402-001 SPEC. INST.[X]	1/2	1/2		2442	3/27/87	1			N/A N/A
	EQUIPMENT# 112								
WAFER SAW 0402-003 SPEC. INST.[X]	1/2	1/2		95	3/31/87	1			N/A N/A
	EQUIPMENT# 0396			50% [ ]		100% [X]			
WAFER CLEAN 0402-002 SPEC. INST.[ ]	1/2	1/2		95	3/31/87	1			N/A N/A
	EQUIPMENT# 1937								
DIE PLATE 0402-004 SPEC. INST.[X]	30	718 30		387	3/31/87	1		[ ] GLASS [X] WAFFLE	N/A N/A
	NOTE: N/A DIE PLATE IF AUTO DIE ATTACH IS TO BE PERFORMED.								
2ND OPTICAL SPEC. INST.[X]	30	30	–	1342	3/31/87	1			N/A N/A
ADDENDUM [ ]	COMMERCIAL:0502-006 [X] MIL. TRANSISTORS/DIODES:(750;2072/73)0502-003 [ ] MILITARY:(883/2010B)0502-007 [ ] OR (883/2010/A)0502-008 [ ]								
[ ]	2ND OPTICAL YIELD/REJECT BREAKDOWN REQUIRED TO SHIP WITH LOT. ACTUAL PROCESS YIELD 100%								
QA ACCEPT 0202-022 SPEC. INST.[ ]	20/30	20/30	–	2569	3/31/87	1	ACCEPT QA IQA		N/A N/A
BACK MARK/CURE 1302-008/003 SPEC. INST.[ ]									N/A N/A
	INDY STANDARD BACKMARK REQUIRED. INK IQA#_____								
DIE ATTACH SPEC. INST.[X]									N/A N/A
	ADHESIVE D/A: 0602-005 [X] EUTECTIC: 0602-007 [ ] EQUIPMENT #_____ DIE MOUNT MAT'L IQA#_____								
[ ]	DIE SHEAR DATA REQUIRED TO SHIP WITH LOT. PKG IQA#_____								

SPLIT LOT

INDY STANDARD PCI - GOLD/TIN

CUSTOMER KRYSALIS CORP.

JOB ORDER # 13054C

ASSEMBLY LOT # 02AA-1 QTY 688

INDY PART # KCANM016S-001A0

CUSTOMER P/N STRUCTURE 1

DIE COUNT/CUST. 30

DIE COUNT/INDY

PKG TYPE/LEAD COUNT SIDEBRAZED/16

MAINTAIN ANTISTATIC PRECAUTIONS

MAINTAIN WAFER LOT I. D.

SHIP BY 4/9/87

DIE SIZE .082 X .056

DIE I.D.#

WAFER LOT # 7076A

ORIGINATOR [signature] DATE 3/26/87 ENG [signature] DATE 3/26/87

REQUIRED MATERIAL:		DESCRIPTION:
PACKAGES	P/N CUSTOMER KIT	.180 X .140
D/A MAT'L	P/N 03-09-0045	84-1 LMI EPOXY ADHESIVE
WIRE	P/N 03-16-0022	(I) 1.25 MIL. AL (BLUE)
O/COAT MAT'L	P/N N/A	
LIDS	P/N 03-07-0006	.365 X .240 COMBO LID
H/SINK & EPOXY/SOLDER	P/N N/A P/N	
PKG/CARRIER LOAD MAT'L	P/N (I)	TUBES
INK	P/N 06-02-0003	MARKEM FRS-7224 WHITE EPOXY

SHIP VIA: FED-X

SPECIAL INSTRUCTIONS:

IF PRODUCT IS RECEIVED IN DIE FORM; N/A ALL DIE PREP PROCESS STEPS EXCEPT 2ND OPTICAL AND Q.A. GATE.

1. WAFER I.D. REQUIRED.
2. ** CAUTION ** DIE ARE UNGLASSIVATED - USE RUBBER TIPPED VACUUM PEN(s) ONLY.
3. WAFER SAW - CUT DIE STRUCTURES PER ATTACHED ILLUSTRATION(s).

INDY CONTROL # 20202767 REV N/C

OPERATION	QUANTITY IN	QUANTITY OUT	QUANTITY REJ	OPERATOR NUMBER	DATE	SFT	QA INSP	REMARKS	ENG OK
PRE WAFER WASH 0402-002 SPEC. INST.[X]									N/A N/A
	EQUIPMENT#_____								
WAFER MOUNT 0402-001 SPEC. INST.[X]									N/A N/A
	EQUIPMENT#_____								
WAFER SAW 0402-003 SPEC. INST.[X]									N/A N/A
	EQUIPMENT#_____ 50% [] 100% [X]								
WAFER CLEAN 0402-002 SPEC. INST.[]									N/A N/A
	EQUIPMENT#_____								
DIE PLATE 0402-004 SPEC. INST.[X]								[] split 0228 from GLASS [X] WAFFLE for 6 mil die	N/A N/A
	NOTE: N/A DIE PLATE IF AUTO DIE ATTACH IS TO BE PERFORMED.								
2ND OPTICAL SPEC. INST.[X]									N/A N/A
ADDENDUM []	COMMERCIAL:0502-006 [X]								
	MIL. TRANSISTORS/DIODES:(750;2072/73)0502-003 []								
	MILITARY:(883/2010B)0502-007 [] OR (883/2010/A)0502-008 []								
[]	2ND OPTICAL YIELD/REJECT BREAKDOWN REQUIRED TO SHIP WITH LOT. ACTUAL PROCESS YIELD _____								
QA ACCEPT 0202-022 SPEC. INST.[]									N/A N/A
BACK MARK/CURE 1302-008/003 SPEC. INST.[]									N/A N/A
	INDY STANDARD BACKMARK REQUIRED. INK IQA#_____								
DIE ATTACH SPEC. INST.[X]									N/A N/A
	ADHESIVE D/A: 0602-005 [X] EUTECTIC: 0602-007 []								
	EQUIPMENT #_____ DIE MOUNT MAT'L IQA#_____								
[]	DIE SHEAR DATA REQUIRED TO SHIP WITH LOT. PKG IQA#_____								

OPERATION	QUANTITY IN	QUANTITY O[illegible]	QUANTITY REJ	OPERATOR NUMBER	DATE	SE[illegible]	QA INSP	REMARKS	ENG OK
PLANT CLEAR.									N/A
0202-025	688	688	0	432	3/31	1	[illegible]		N/A
SPEC. INST.[]									

PCI REVISION HISTORY:

ORIGINATED: 03/26/87

5/12/87

7

Mr. John Sheets
Process Engineer
ASM America, Inc.
4302 E. Broadway
Phoenix, Arizona 85040

Dear Mr. Sheets,

On the 18th of March of this year, we met to discuss the evaluation of a top passivation process. After several delays, the samples have been prepared to complete the test matrix.

The test matrix discussed was as follows:

A six way split with three different film sandwiches and two different process temperatures was the final form of the test matrix.

film sandwich	process temperature (C)
0.75 microns, NITRIDE	300
0.75 microns, NITRIDE	380
0.25 microns, OXIDE capped with 0.50 microns, NITRIDE	300
0.25 microns, OXIDE capped with 0.50 microns, NITRIDE	380
0.25 microns, OXIDE capped with 0.50 microns, OXYNITRIDE	300
0.25 microns, OXIDE capped with 0.50 microns, OXYNITRIDE	380

Other process details:

thin film	film stress
OXIDE	~4×10^9
NITRIDE	~6×10^9 (Lo Compressive)
OXYNITRIDE	~10^8 (Mildly Compressive)

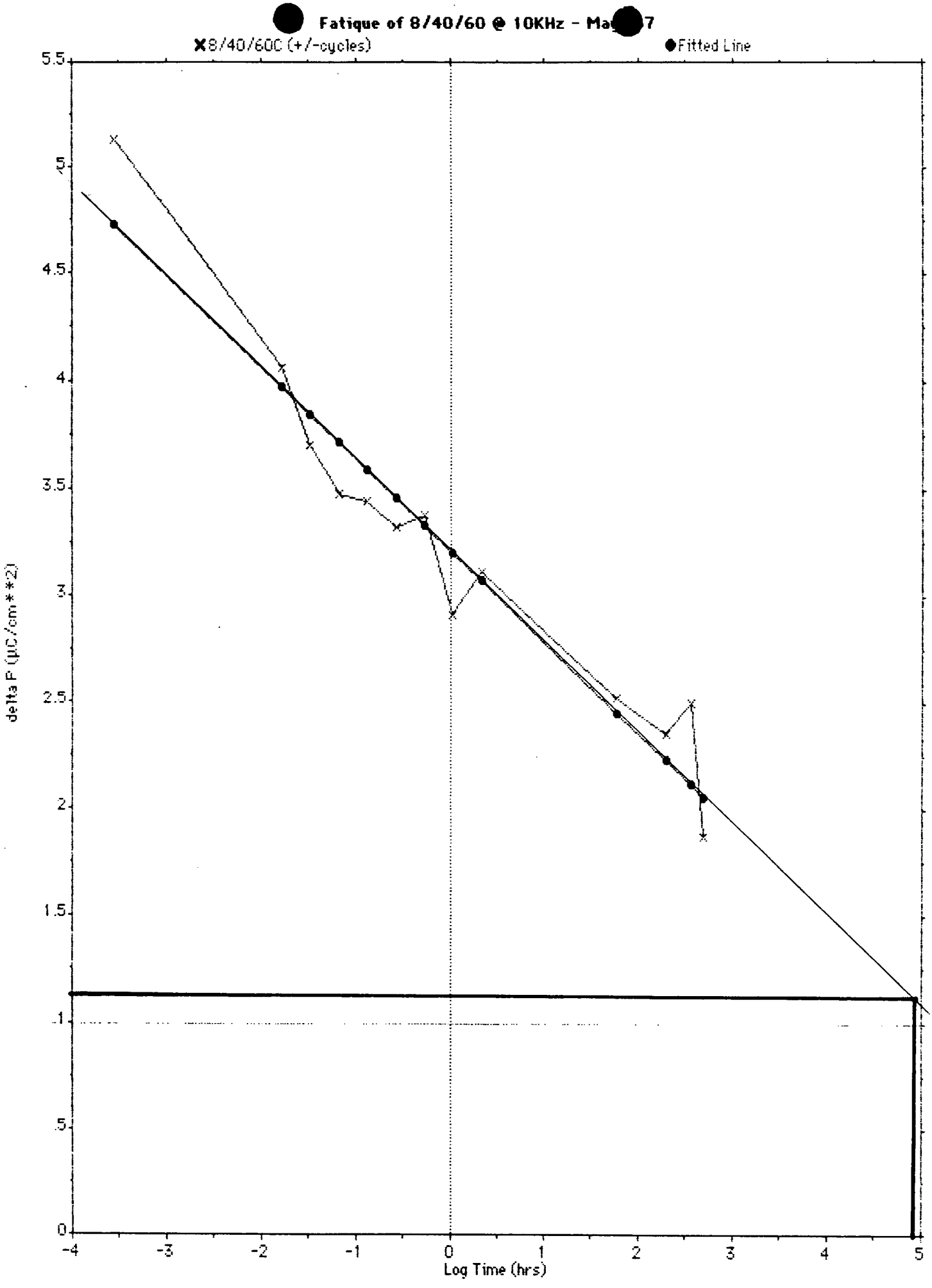
thin film	refractive index
OXYNTRIDE	~1.8

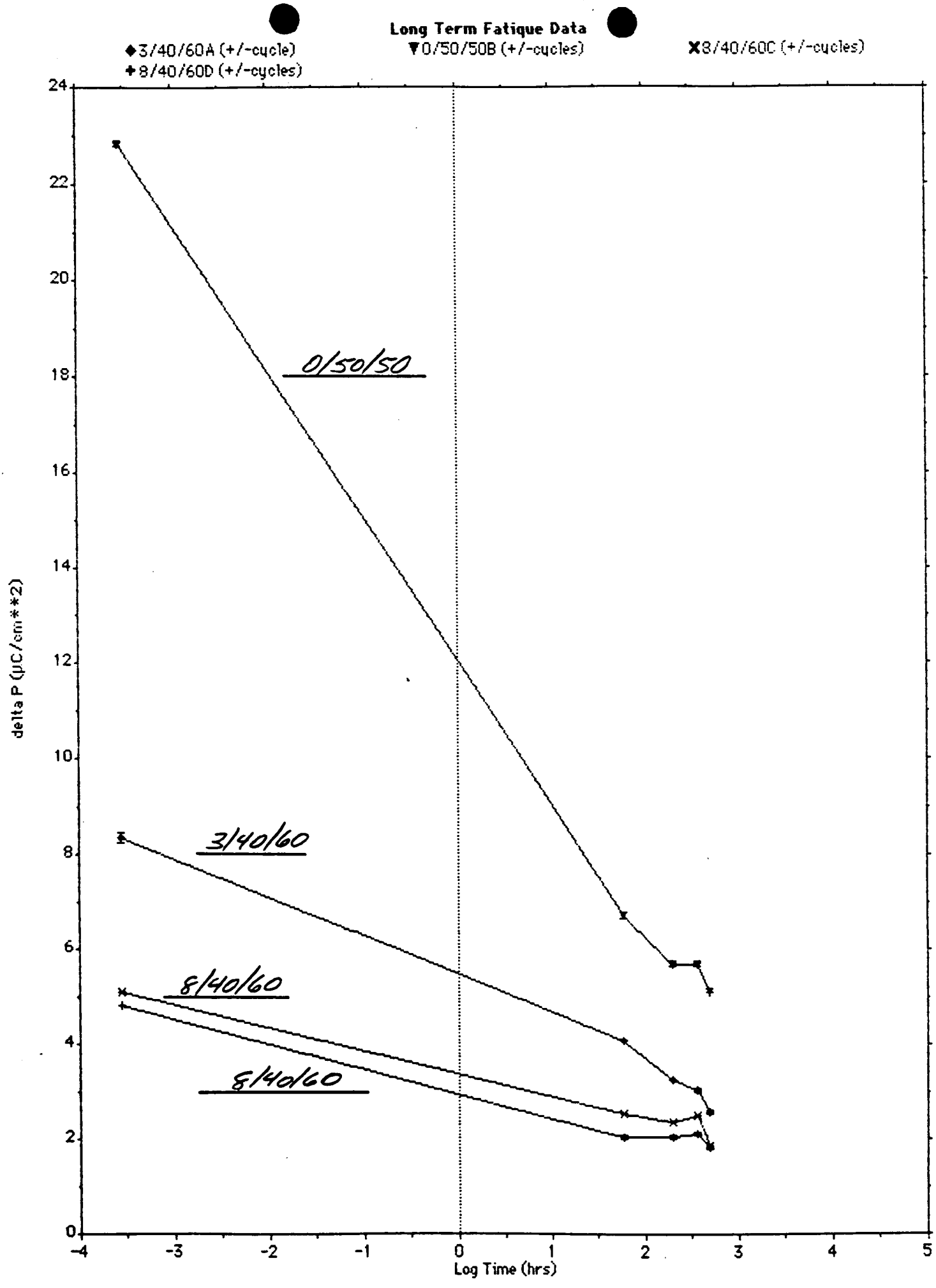
The 12 test wafers will accompany this letter. An ID# has been scribed on the backside of each wafer. If you require any addition information, or wish to discuss the test matrix outlined above, I can be contacted at either (505) 345-1953 (office), or (505) 277-1429 (lab).

Sincerely,

Dino Asselanis
Process Development
Engineer

C.C. Bill Miller
Bill Shepherd


[redacted] Fatique of 8/40/60 @ 10KHz - Ma[redacted]7
X8/40/60C (+/-cycles)
Fitted Line
delta P (µC/cm**2)
Log Time (hrs)
5.5
5
4.5
4
3.5
3
2.5
2
1.5
1
.5
0
-4
-3
-2
-1
0
1
2
3
4
5


Long Term Fatique Data
◆3/40/60A (+/-cycle)
▼0/50/50B (+/-cycles)
✖8/40/60C (+/-cycles)
✚8/40/60D (+/-cycles)
0/50/50
3/40/60
8/40/60
8/40/60
delta P (µC/cm**2)
Log Time (hrs)
24
22
20
18
16
14
12
10
8
6
4
2
0
-4
-3
-2
-1
0
1
2
3
4
5

Confidential
Krysalis Corporation

To: Franc deWeeger
From: Bill Miller
Date: June 22, 1987
Subject: Technology Development Action Plan

This plan's objective is to maximize our chances of producing a rel qualified 16K on schedule. To meet this objective we must anticipate and pro-actively address potential reliability problems and accelerate our materials research and process development programs. Boundary conditions include financial limitations and the limited rate at which we can effectively identify, hire, and indoctrinate new people. The plan presented below is the result of discussions with Wayne Kinney and Bill Shepherd concerning this objective. I believe the consensus opinion is that we are not currently throwing enough resources at the problem to effectively anticipate and evaluate the issues and supply solutions at the rate which will result in a high probability of success. Much of this plan is directed at adding enough people to adequately cover the issues and support the level of activity needed to give us a shot at successfully meeting the schedule.

Ferroelectric Storage Capacitor

Wayne Kinney will direct the ferroelectric capacitor development, characterization, and research program.

Issues -

1) We don't understand fatique and we do not have much confidence in a pediction of ten years operating life based on extrapolation of data collected to date.

2) The material that looks best in terms of fatique has problems with microstructure and possibly TDDB

3) Much more in the way of electrical characterization is needed to pick out additional potential problems.

4) We need to improve our understanding of process effects and develop process control procedures for the ferroelectric materials.

Actions -

1) Beef up electrical properties characterization efforts to increase the rate of development of phenomelogical understanding

Current efforts-

- Long Term Fatigue Characterization
- TDDB Characterization
- Retention experiments

Planned efforts -

- Cross correlation of measurement systems
- Identification and elimination of sources of systematic measurement error
- Development of improved methodology and software to increase characterization and analysis efficiency
- Characterization over a broader range of conditions
- Addition of equipment for improved quick turn sample packaging
- Addition of personnel to increase through-put and support characterization for a higher rate of ferroelectric capacitor processing and compositions experiments

2) Add an effort specifically aimed at improving and controlling the ferroelectric films deposition technology.

Planned Efforts -

- Process chemistry variations
- Drying/Anneal temperature cycle variations
- Drying/Anneal ambient variations
- Process control issues and methods

3) Beef-up efforts in experimental and theoretical materials science to increase the rate of developing an understanding of the mechanisms for observed variations and changes in materials properties with special emphasis on fatique.

Current Efforts-

- University of Illinois contract for physical characterization of capacitors
- Contract with UNM for modeling polarization mechanisms in ferroelectrics

Planned efforts-

- Additional university contracts focused at theory and modeling of ferroelectric properties
- Extensive physical characterization with a variety of tools

Current Personnel -

Wayne Kinney will work on the development of an understanding of the physical mechanisms which lead to observed properties of the ferroelectric materials in parallel with his general program management responsibility

Mike Cordoba, who will assume product engineering responsibility after first 16K

silicon becomes available, will continue to work on LTF/STF and retention experiments. Some of this load will be allocated to new personnel as they become available.

Anita Navarro will continue to support hardware development, LTF/STF organization/clerical requirements, and measurements.

Additional Personnel -

Engineer/Scientist (ferroelectric films processing)
Engineer (electrical characterization - hardware development, experimental design, experimental execution, and data analysis)
Technician (ferroelectric films processing support)
Technician (electrical characterization organization/clerical, measurement, and hardware development activities)
Technician (sample preparation and physical analysis)

Process Development

Bill Shepherd will direct the process development program exclusive of the issues concerning the properties of the ferroelectric capacitor.

Issues-

1) Potential for latent migration of contaminants carried by the ferroelectric capacitor fabrication process which lead to shifts in semiconductor device characterisitics during reliability testing.

2) Potential for problems with materials interfaces which have not been used in the past in any application. These include:

- Bottom Electrode to Ferroelectric
- Top Electrode to Ferroelectric
- Top Electrode to Interlevel Dielectric - 2
- Aluminum Interconnect to Barrier to Top Electrode
- Aluminum Interconnect to Barrier to Silicon Junctions

3) Our ability to produce 16K like structures for reliability evaluation is limited because some of the K16 process elements have not yet been developed (ILD, dry etch Aluminum, and passivation process elements).

Actions-

1) Write specs and add operators to support standard wafer processing in order to free engineers to focus on yet to be done process development and on potential reliability issues.

2) Accelerate development of planned 16K process elements including ILD, Al etch, and passivation.

Current Efforts-

- Silox ILD and passivation experiments
- Initial Nitride and Oxynitride passivation experiments
- Dry etch equipment selection

Planned Efforts-

- ILD and passivation deposition equipment selection
- Al dry etch process development

3) Accelerate reliability experiments using test structures and devices focused at each of the anticipated failure modes or potential problem interfaces.

Planned Efforts-

- BHTL and 85/85 on 512 with passivation and ILD
- BHTL and 85/85 LTF with ILD test structures
- Failure analysis and problem identification

4) Add a metallurgist to the staff to focus on potential metal interface problems and solutions.

- Electromigration in AL/PT contact strings
- Corrosion in Al/Pt contact strings
- Alternative barriers
- Reliability of AL/PT/N+ strings

Current Personnel-

Bill Shepherd/ Program Director

Dino Asselanis/Process Engineering (lithography)
Harry Suh / Process Development (dry etch, metals, dielectrics)

Leo Chapin/Process Development (FE films dep, SEM)
Alan Figuracio/Wafer Fab (lead operator/supervisor)

Additional Personnel-

Reliability Engineer/Scientist (failure anticipation, test definition, failure analysis)
Process Development Engineer/Scientist (Metallurgist)
Process Engineer (Wafer Fab Support)
Reliability Tech (hardware development, logistics, set-up, execution)
(2) Process Development Techs
(3) Wafer Fab Operators

Electrical Tests to be Supported

Standard LTF

- 3 compositions
  - 8/40/60
  - 0/50/50
  - 3/40/60
- 30 packages of each composition with no Al on FES
- 6 packages of each composition with Al on FES

Consider 15/0/100 in extra sockets as packaged caps are available

Experiments in Fatigue vs. Composition and Structure

Fatigue vs. Thickness

- 4 compositions
  - 8/40/60
  - 3/40/60
  - 0/50/50
  - 6/50/50
- 2 thickness layers
  - 4 layers
  - 16 layers
  - Do 8 layer wafer for 0/50/50 also

Buffer layers vs Fatigue

- First and last layers 15/0/100
- 4 compositions, 6 middle layers (8 total layers for each capacitor)
  - 8/40/60
  - 3/40/60
  - 0/50/50
  - 6/50/50

Hybrid Gel Experiment

- 3/40/60 from 15/0/100 and 0/50/50, 8 layers
- ?/80/20 from same if 3/40/60 works, 8 layers

If hybrid gel experiment works, consider the following compositions:

- 0/40/60
- 6/50/50
- 8/0/100
- 0/20/80
- 8/20/80

Critical Issues to Study

Caps over topology - redesign 512 immediately to look at 16K cell

Effect of duty cycle on fatigue of film

Disturb phenomenon in continuous FES

CMOS contact resistance using TD01 wafers

dP worst case for data reliability

Ps max or RATL max

Worst case Step dP vs. Pulse dP

DC fatigue

TDDB

Effective threshold vs. number of disturbs

Signal vs pulsewidth

TEL over BEL edge

Al over TEL

Retention

Polarization vs. thickness and field

Disturb pulses

Define "standard" and "exotic" FES measurements

PEM design

Fatigue vs. Voltage scale, temperature, process, structure

Passivation

Curie point meaasurements and polarization vs. temperature measurements

Physical characterization (SEM, X-ray, TEM, etc.)

Theory

512

- Test
- Iterations
- Reliability
- Performance
- 3 line control

16K

- Design schedule
- Architecture
- Performance
- Reliability
- Topology

An Experimental 512-Bit Nonvolatile Memory with Ferroelectric Storage Cell

Richard Womack, Wayne Kinney, Bill Shepherd, Bill Miller, and Joe Evans

Krysalis Corporation

4200 Balloon Park Road NE

Albuquerque, New Mexico 87109

(505) 345-1953

Krysalis Corporation has succeeded in fabricating an experimental 512-bit random access memory based on ferroelectric capacitor storage cells. The device was designed solely for use in process development and electrical characterization and includes on-board test circuitry for that purpose. The internal timing of the memory is controlled externally to allow experimentation with timing algorithms. The memory is referred to as the 512 Externally Controlled Device, or 512 ECD, because of the timing interface. See Table 1 for the device statistics and Figure 1 for the die photograph.

The device uses the natural remnant polarization of ferroelectric capacitors to store digital data states. The memory cell consists of a pass transistor/ferroelectric capacitor combination (Figure 2). The ferroelectric capacitors have been demonstrated to switch in less than 5 nanoseconds allowing the nonvolatile cell to be written or read directly during a memory access. The memory functions as a static RAM where every access is nonvolatile.

A ferroelectric capacitor has a highly non-linear dielectric with a hysteresis in the capacitance plot of charge vs. voltage (Figure 3). Unlike a DRAM storage capacitor, charge remains in the capacitor at zero applied

volts. The remnant charge stored in the ferroelectric capacitor requires no refresh. Therein lies the usefulness of the ferroelectric capacitor as the nonvolatile storage medium.

The 512 ECD uses a double-ended sense scheme to create a self-referencing signal differential across the sense amp. A block diagram is shown in Figure 3. The memory bit consists of a word line (WL) controlling two pass transistors, a bit line (BL) and a bitbar line (BLb) to collect charge from the capacitors, and a common drive line (DL) to actively drive the capacitors. A sense amp resides between BL and BLb. For a write, the sense amp is set to the desired state and BL and BLb are driven to the opposite voltage values of V_{drive} and ground. The DL is pulsed in such a way that the high DL against the grounded bit line writes the Q(0) state into its capacitor. When the DL drops to ground after the pulse, the other capacitor has a Q(1) written in it by its high bit line voltage.

The read operation is best understood by examining the photograph of the BL signals in Figure 4. A voltage step is applied to DL with the bit lines floating and the sense amp off. Since the capacitors are in opposite states, BL and BLb will collect different amounts of charge and produce a voltage differential of a polarity determined by the stored data. The sense amp then turns on to capture the datum. With the sense amp on, the bit lines are driven to the opposite rails and the destructively read datum is automatically restored. The restore is invisible to the user and occurs in parallel with the output gating of the read data to the I/O ports. Note the 1- volt differential generated on the bit lines by the two capacitor states.

The internal organization of the 512 ECD is shown in the Figure 1 overlay. The device is arranged as a 64 x 8 memory. The memory array consists of 64 rows of 8 bits apiece with no column decode. One row consists of 16 capacitors sharing a common WL and DL and arranged as 8 double-ended memory bits.

The capacitors are approximately 5μ by 9μ, less than 1μ thick, and have a nominal capacitance of 1 picofarad apiece. The DL drivers and WL drivers are located on either side of the memory array. Regenerative feedback amplifiers similar to those in DRAMs constitute the sense amps. The device has standard three-state I/O functions.

The WL, DL, sense amp, and equalization functions are controlled from buffered inputs. In combination with the I/O controls, the 512 ECD requires seven timing inputs to actively control the device in normal operation. The seven control lines are unique to the 512 ECD. Products based on this technology may be designed with standard SRAM three-line control.

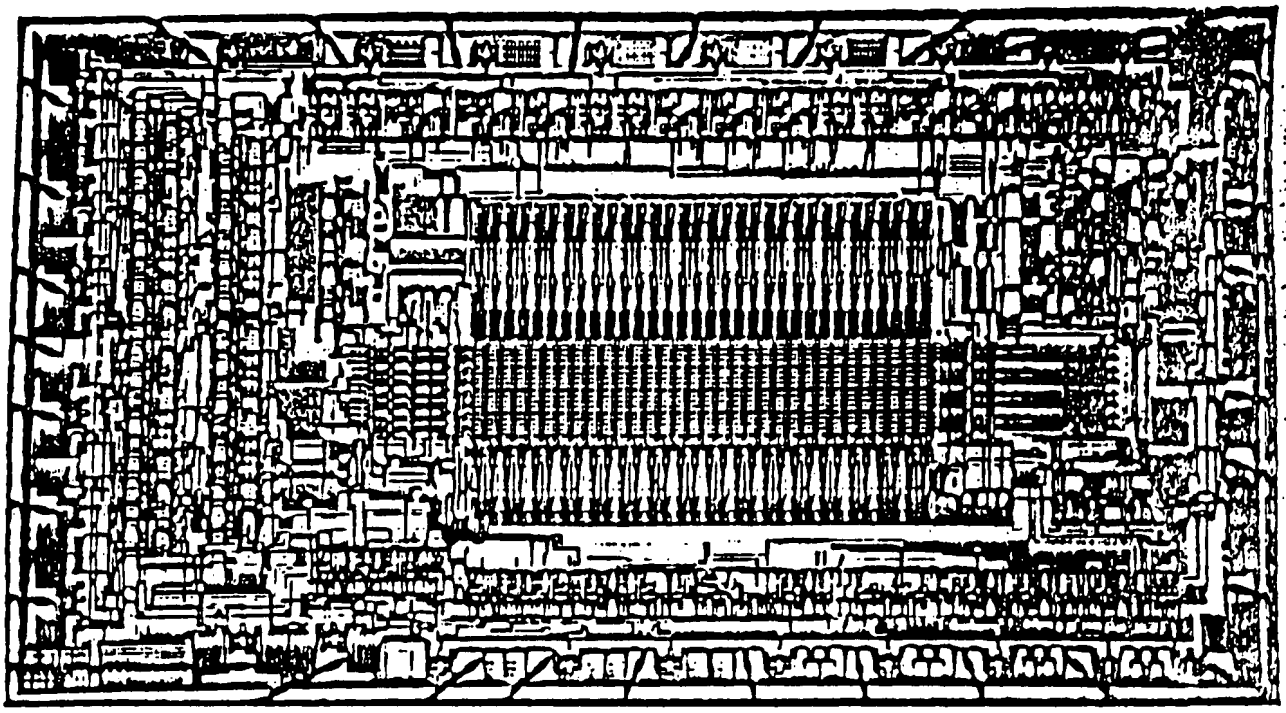
The top 20% of the die is occupied by special analog test circuitry consisting of source followers connected to the bit lines. Computer controlled analog to digital converters are used to capture the BL voltages resulting from a DL pulse applied to the ferroelectric capacitors on a row. The system allows the study of capacitor performance in the integrated circuit over a wide range of operating conditions.

The 512 ECD program has proven highly successful. The capacitors have demonstrated the ability to be scaled to as small as 3μ x 3μ while still maintaining strong signal levels. Access times for future designs may drop well below the 100ns mark. The fundamental design concepts of the 512 ECD have been validated and design and process rules for larger and more space efficient memories have been generated.

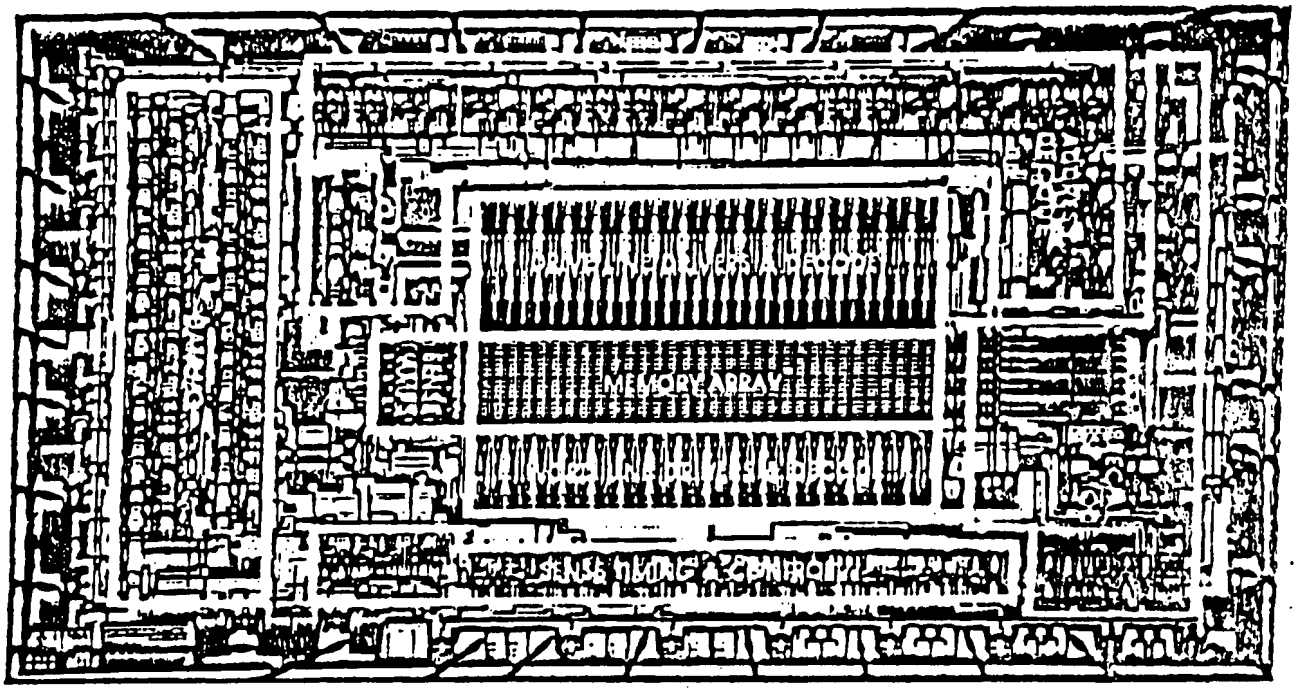
Table 1
Critical Statistics

Technology	N-well CMOS
Critical Feature Size	3 micron
Die size	3.2mm x 6mm
Power Supplies	5 volts, 7.5 - > 10 volts
Active Power	40mW
Cell Size	1300 μ^2
Capacitor Size	5μ x 9μ
Read/Write Access Speed	550ns
Tested Read Accesses per byte (50°C)	10^{12}
Projected Read Accesses per byte (50°C)	$>10^{15}$
Tested Write Accesses per byte (50°C)	10^{11}
Projected Write Accesses per byte (50°C)	$>10^{12}$

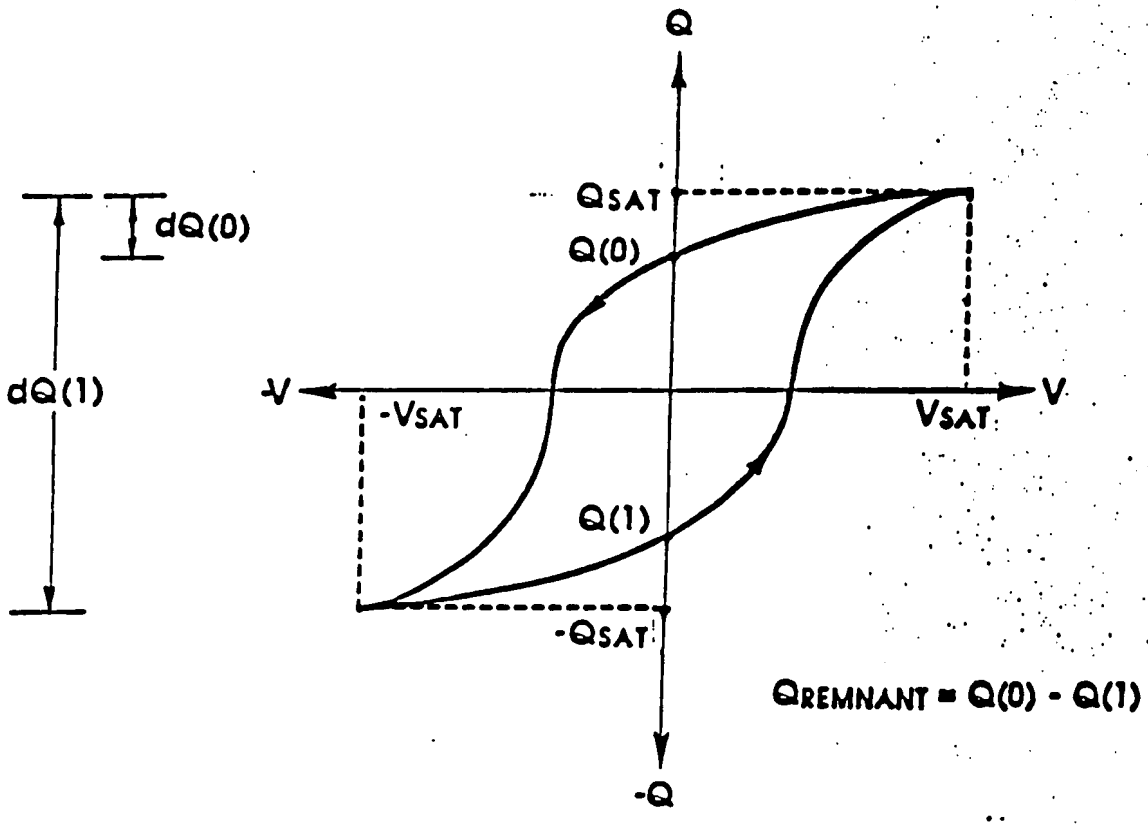
Figure 1



512 ECD

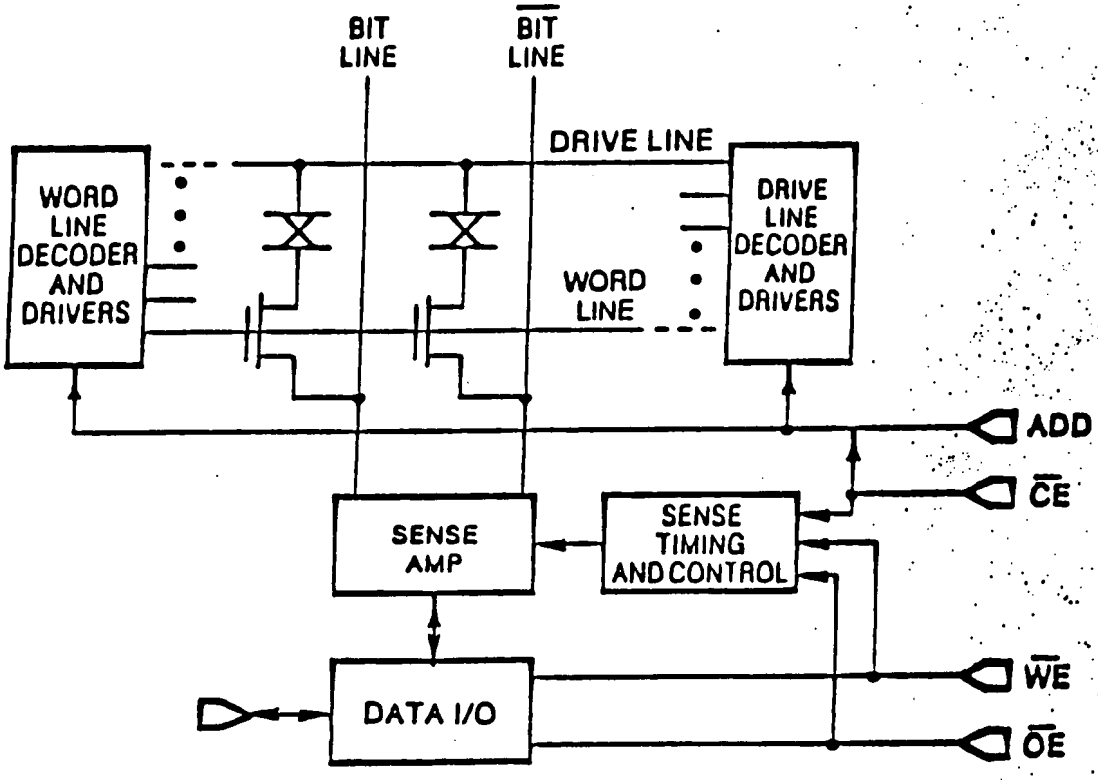


512 ECD Internal Organization



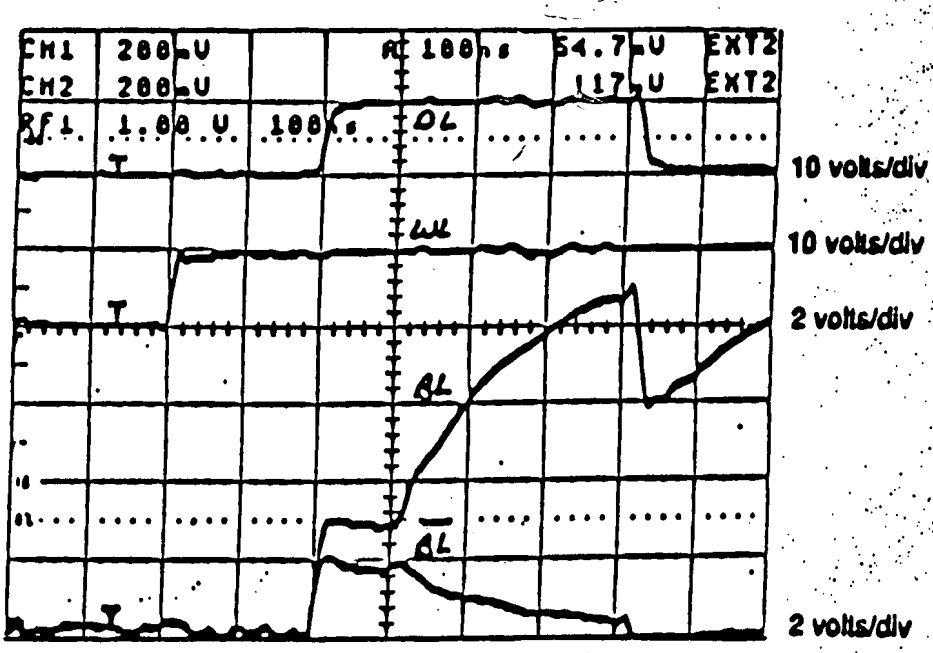
Memory cell showing remnant polarization of the ferroelectric capacitor.

Figure 2



512 ECD Block Diagram

Figure 3



Photograph showing voltage applied to DL with the bit lines floating and the sense amp off.

Figure 4.